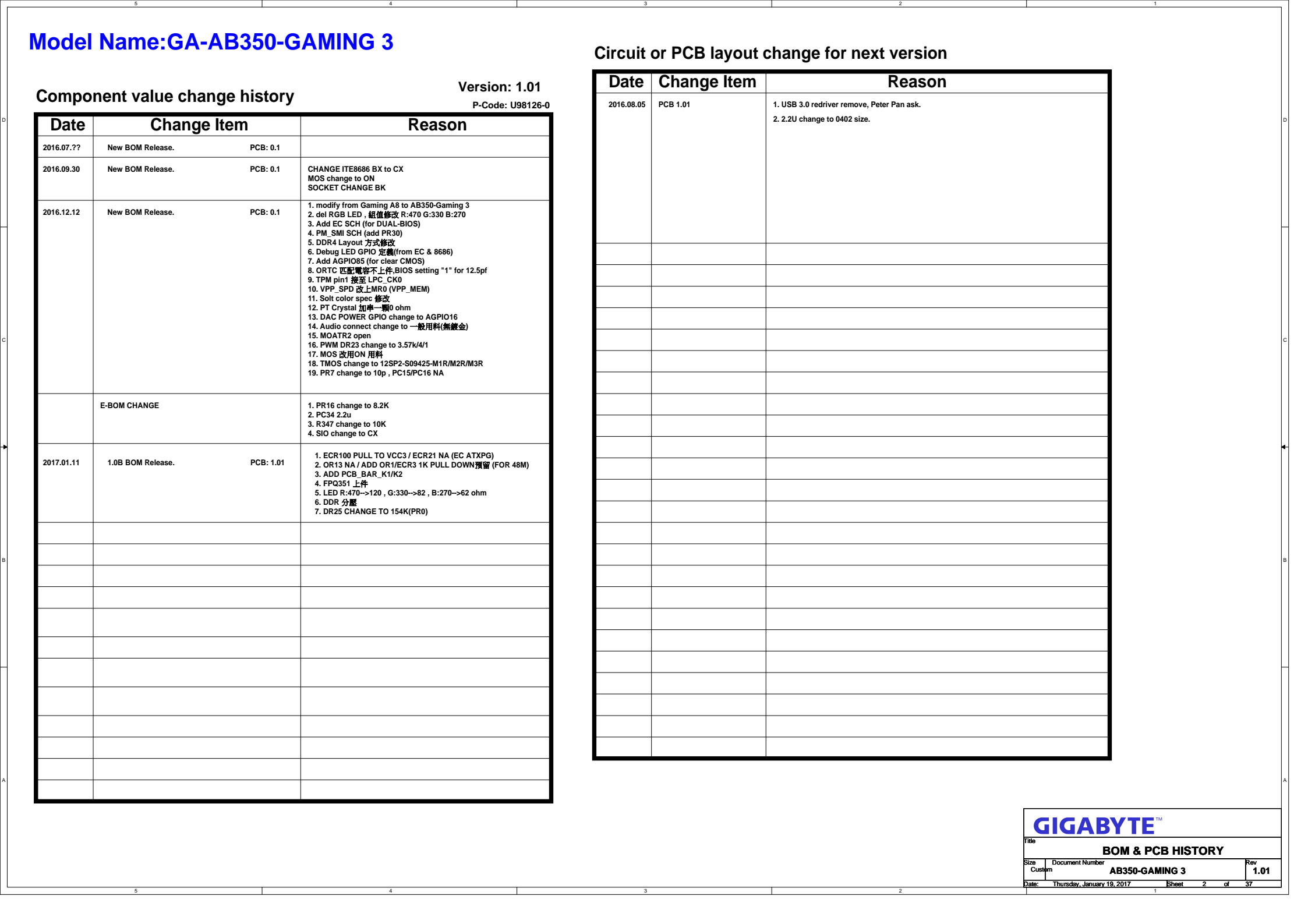
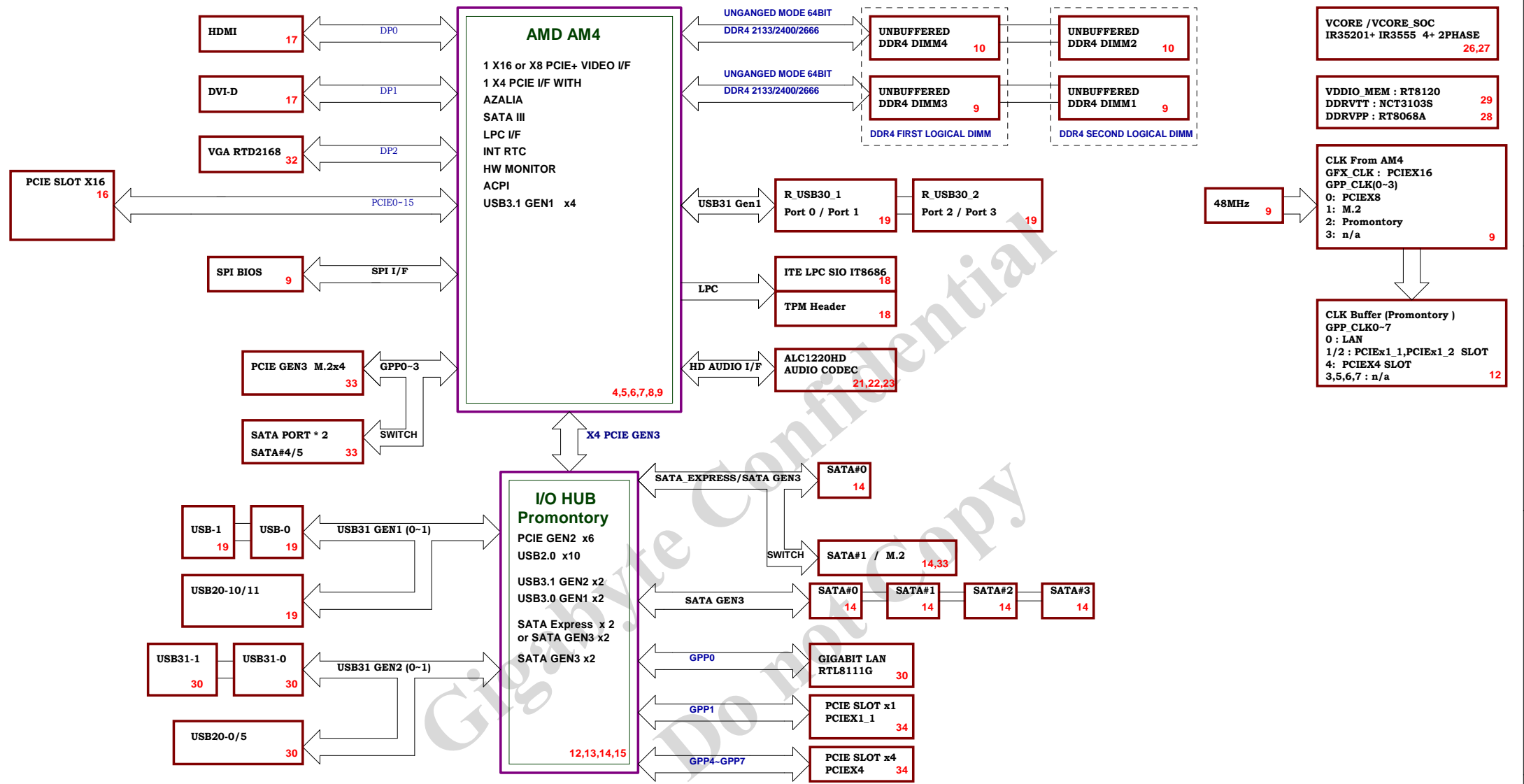


GA-AB350-GAMING 3

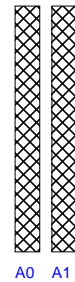
PAGE	TITLE	Revision : 1.01
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK, SPI, MISC	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	HDMI , DVI	
18	IT8688CX , TPM	
19	F_USB30 , R_USB30 , F_USB20	
20	A_VDD1V8, DAC_PWR	
21	ALC1220 CODEC	
22	AUDIO JACK	
23	POWER SEQUENCE , A_VDDP	
24	PWM SL95712	
25	VCORE MOS , VCORE_SOC MOS	

[illegible]

[illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible][illegible]

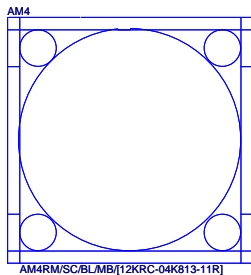


MEM CHA



<10> MODT_A[0..3] ↔ MODT_A[0..3]
<10> MDA[0..63] ↔ MDA[0..63]
<10> MAA[A0..16] ↔ MAA[A0..16]

<10> DQSA[0..7] ↔ DQSA[0..7]
<10> -DQSA[0..7] ↔ -DQSA[0..7]



<11> MODT_B[0..3] ↔ MODT_B[0..3]
<11> MDB[0..63] ↔ MDB[0..63]
<11> MAAB[0..16] ↔ MAAB[0..16]

<11> DQSB[0..7] ↔ DQSB[0..7]
<11> -DQSB[0..7] ↔ -DQSB[0..7]

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Title					
APU DDR4					
Size	Document Number				Rev
Custom	AB350-GAMING 3				1.01
Date:	Thursday, January 19, 2017		Sheet	4	of 37

A0 A1

A

AM4RM/SC/BLMB[12KRC-04K813-11R]

A

D

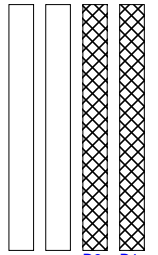
D

C

C

B

MEM CHB

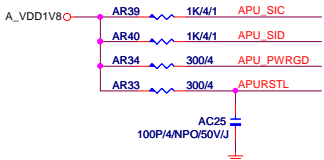


B0 B1

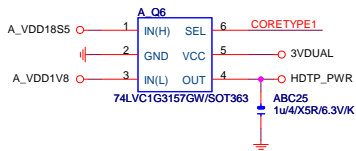
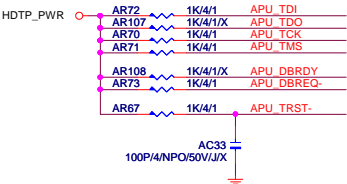
B

A

A

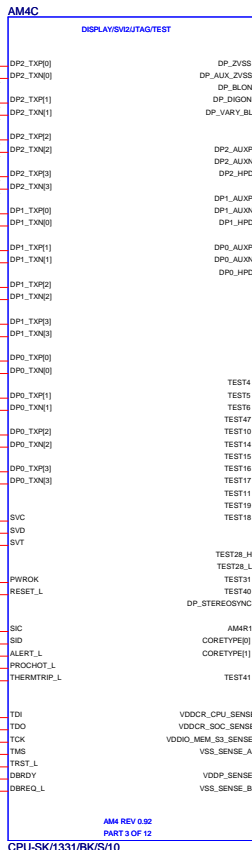
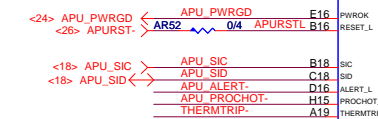
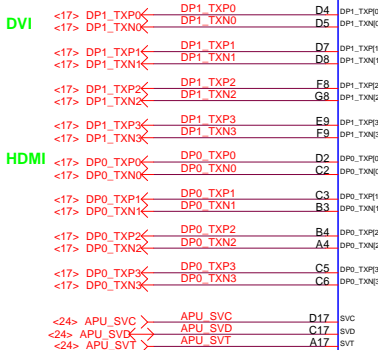


SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

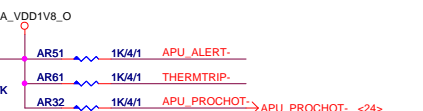
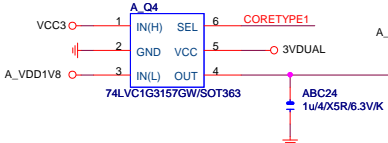
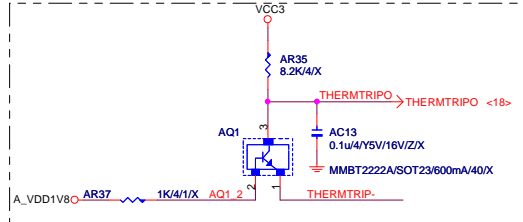
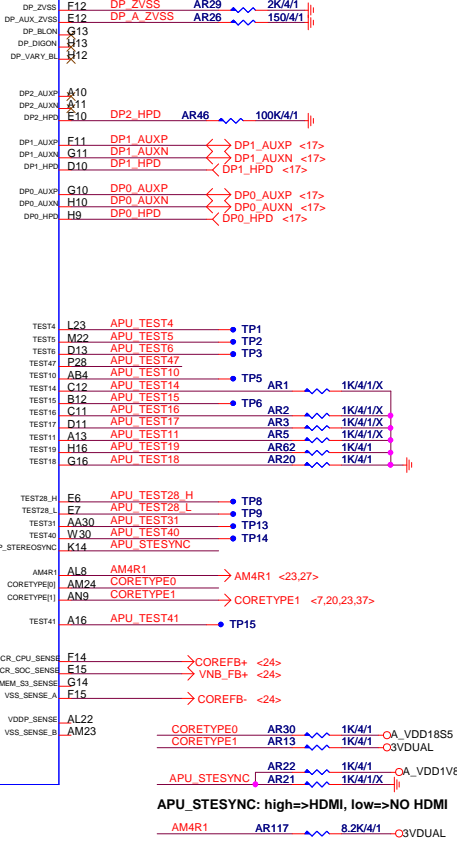


DVI

HDMI



Placed within 1500 mils from APU



AM4 CPU CoreType

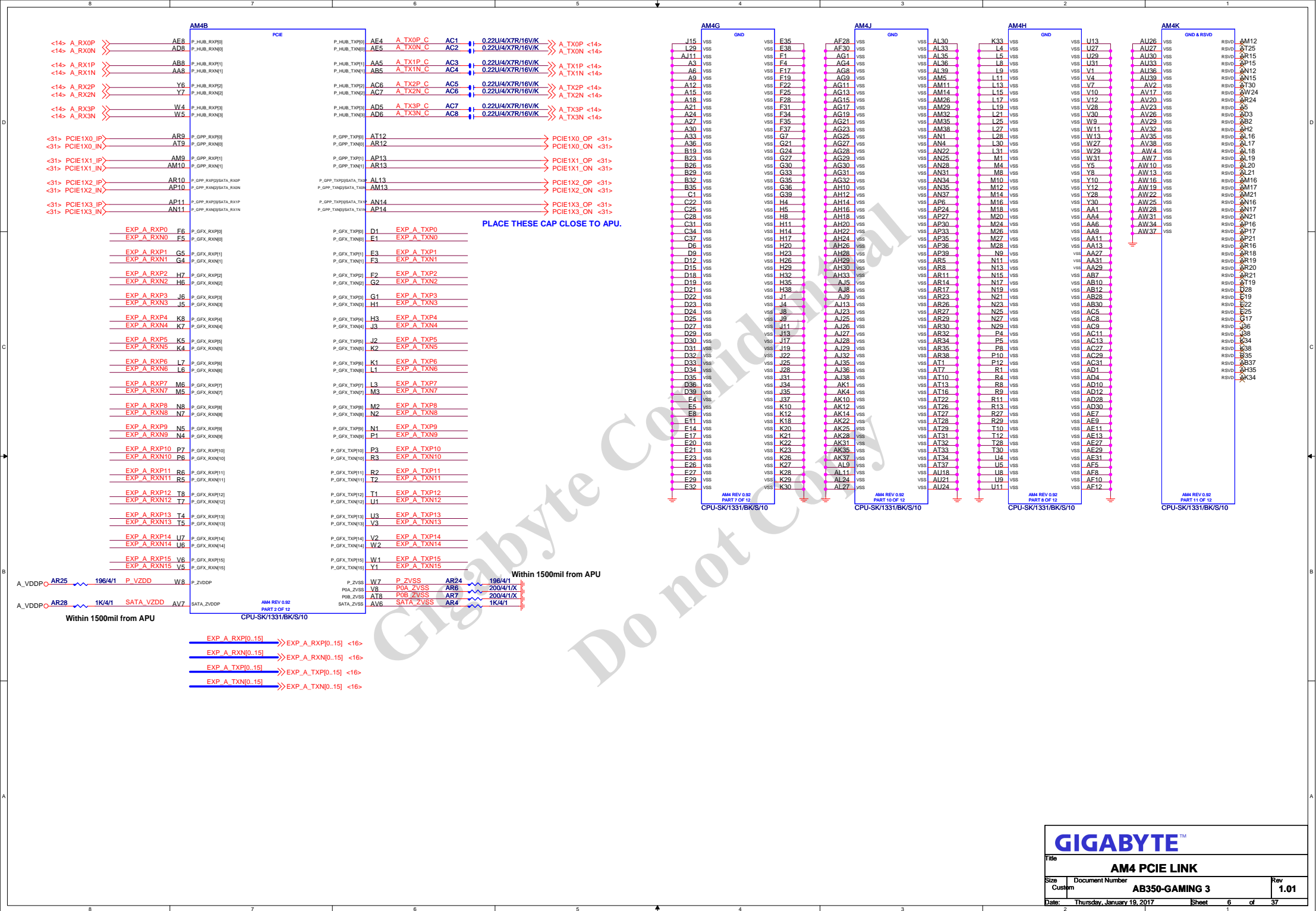
CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

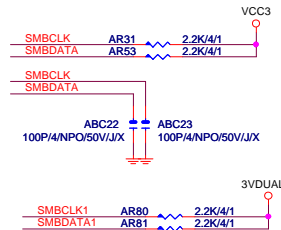
GIGABYTE™

Title: **CPU CONTROL**

Size: Custom Document Number: **AB350-GAMING 3** Rev: **1.01**

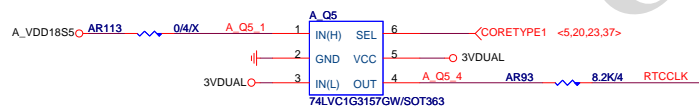
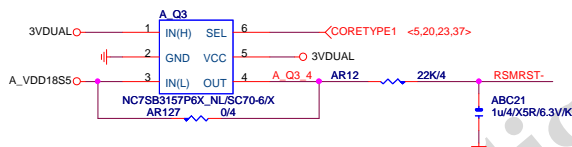
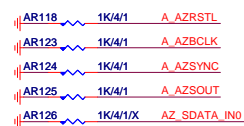
Date: Thursday, January 19, 2017 Sheet: 5 of 37



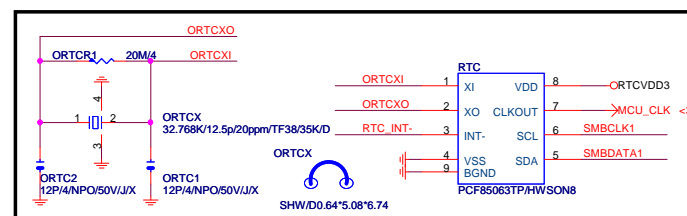


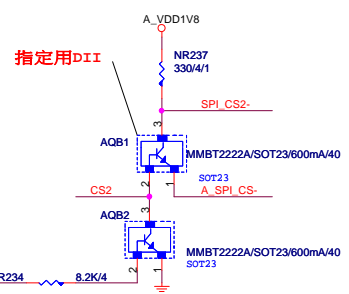
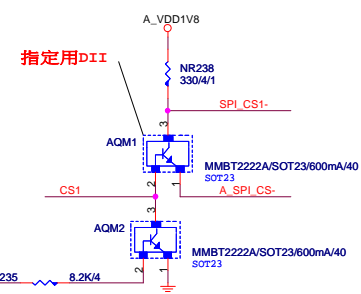
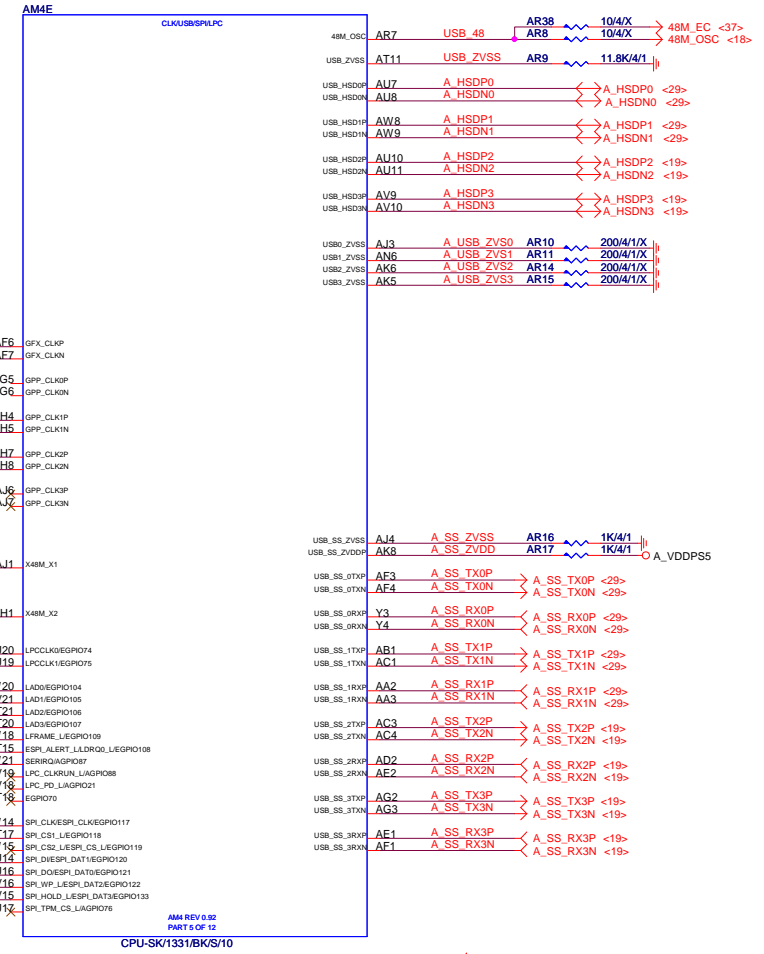
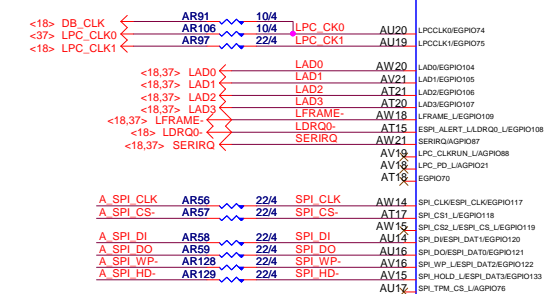
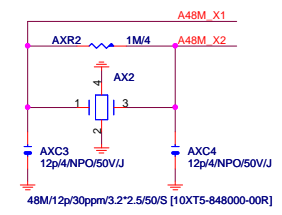
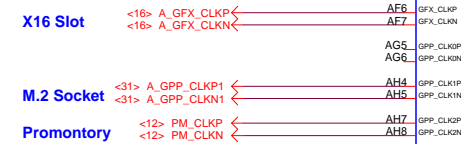
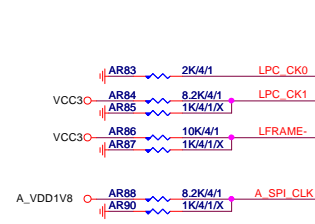
Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

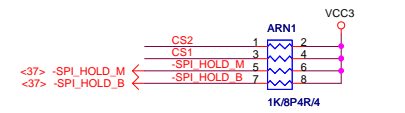
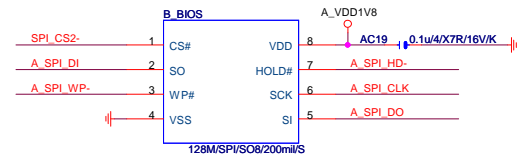
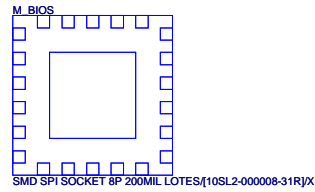
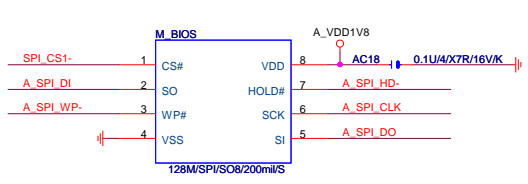
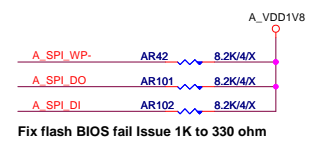


	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI_CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48MHz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100MHz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic	Coin battery is not on board.	LPC ROM	short reset mode	Use 100MHz PCIE clock as reference clock and generate internal clocks only
	CE/ST DIE ONLY						ZP DIE ONLY





★1.8V SPI ROM USE

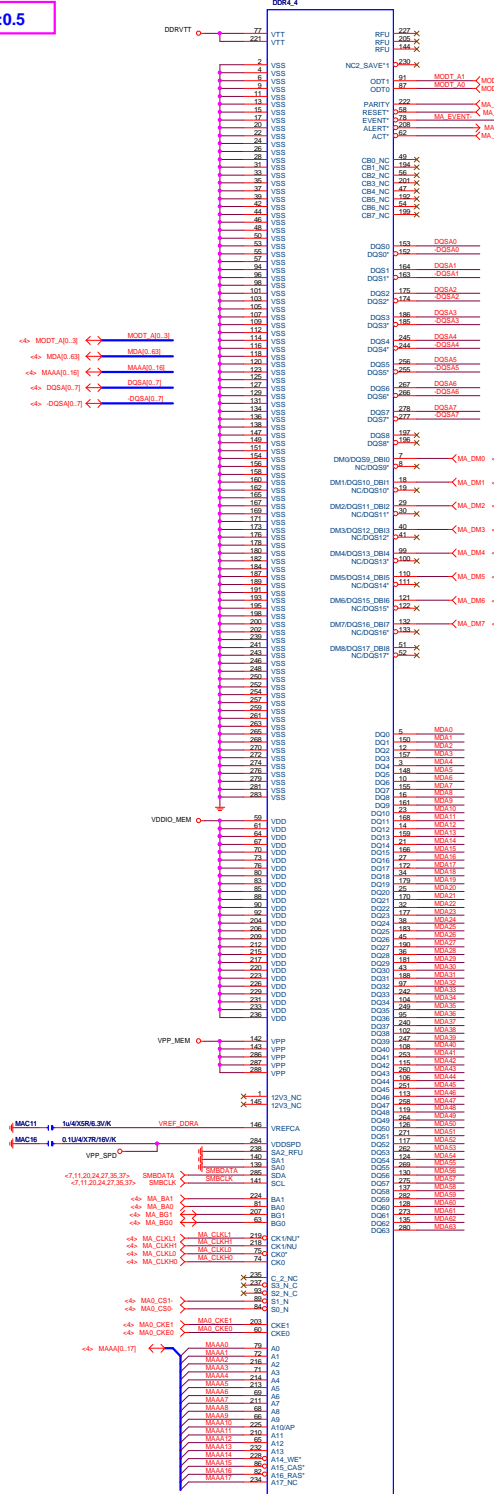


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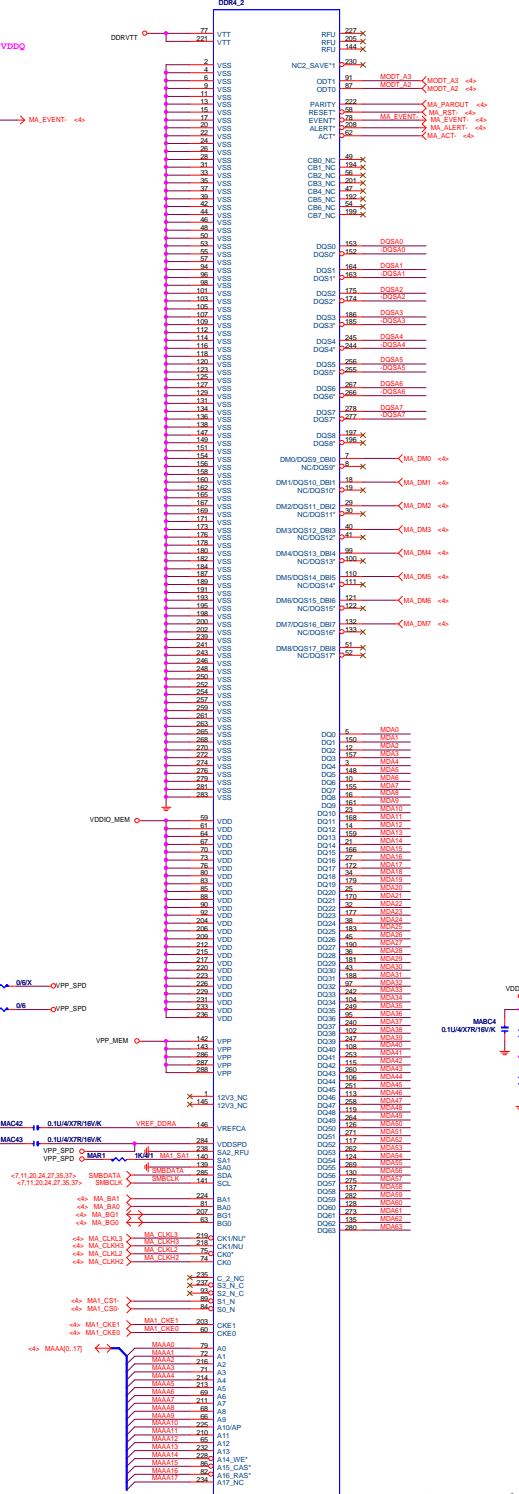
Title **DDR4 CHANNEL A**

Size Custom Document Number **AB350-GAMING 3** Rev **1.01**

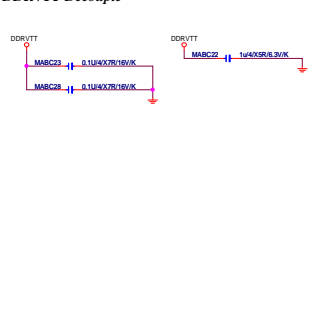
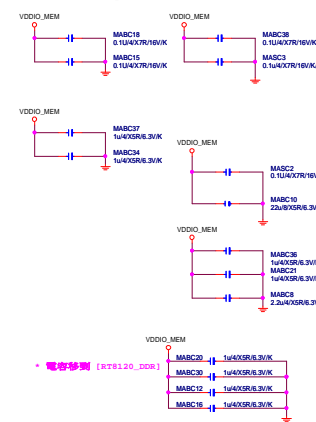
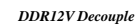
Date: Thursday, January 19, 2017 Sheet 9 of 37

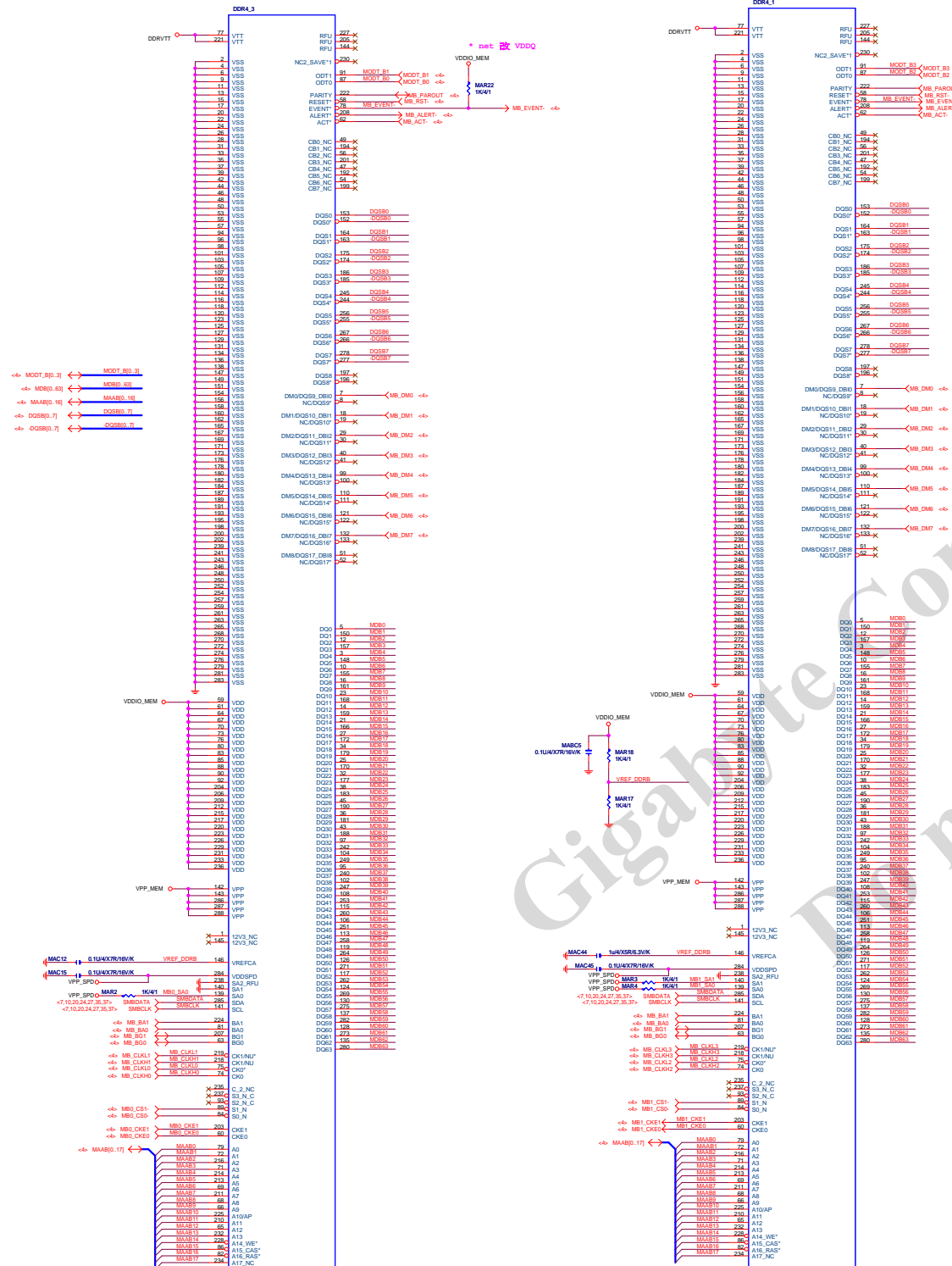


CHANNEL A0
SA2:0=000



CHANNEL A1
SA2:2=010



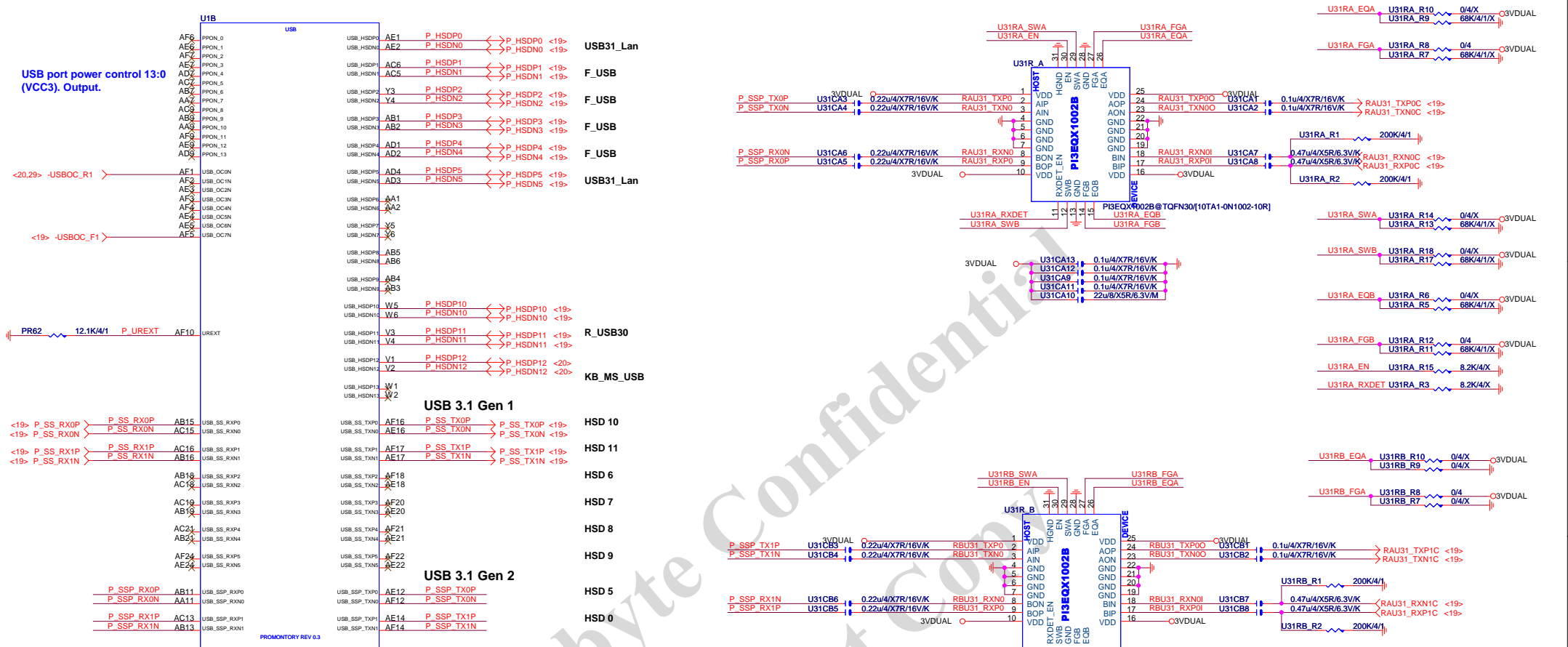


CHANNEL B0
SA2:1=001



CHANNEL B1
SA2:3=011





USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

ANS 5133386

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Title

B350 USB , PI3EQX1002B

Size

Document Number

AB350-GAMING 3

Rev

1.01

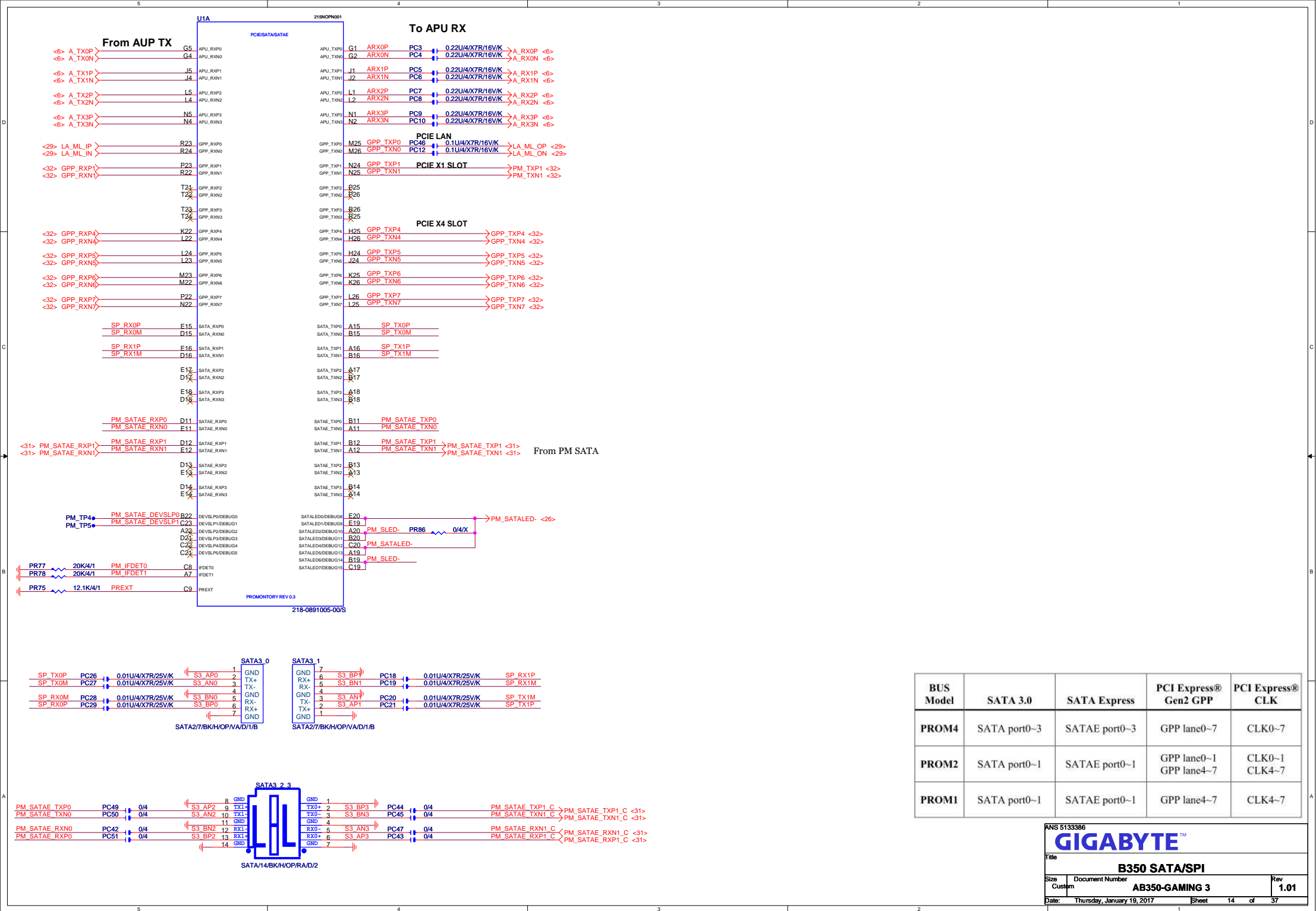
Date: Thursday, January 19, 2017

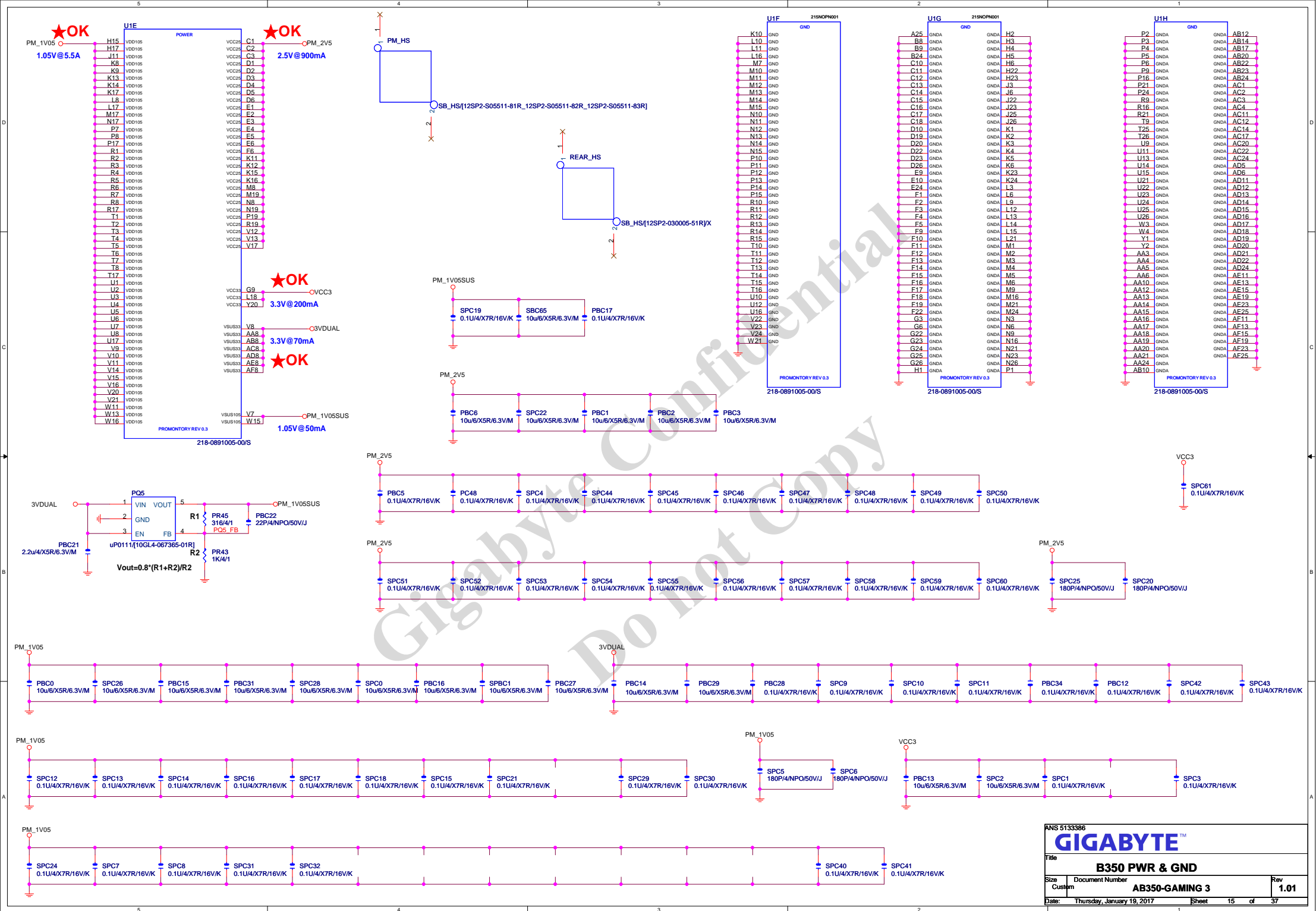
Sheet

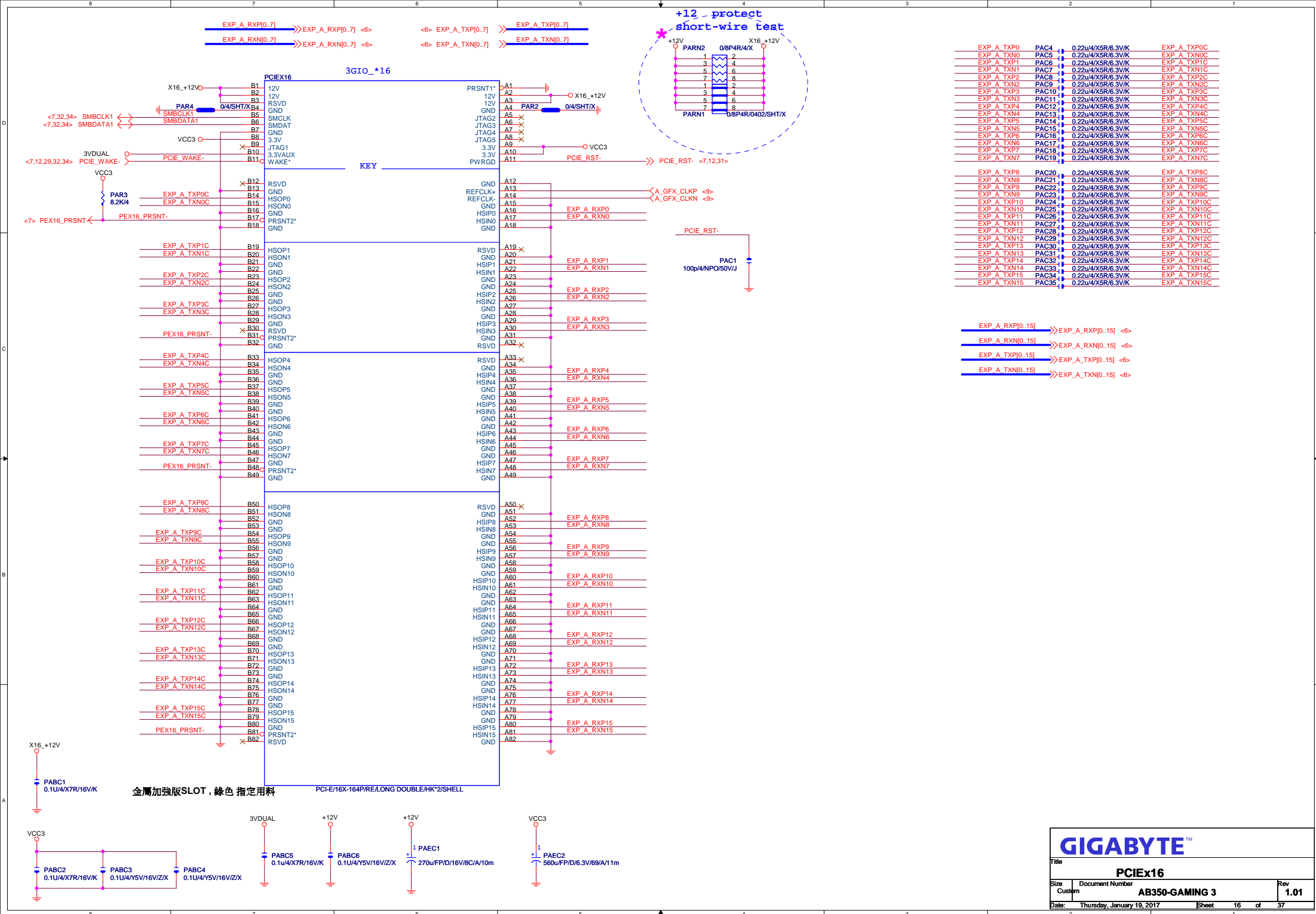
13

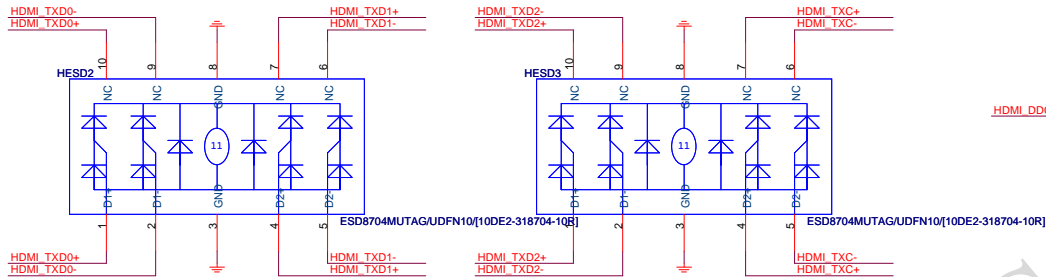
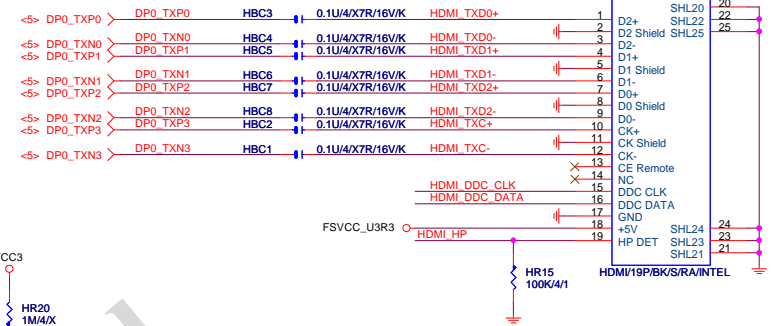
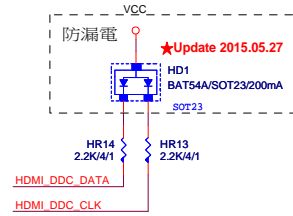
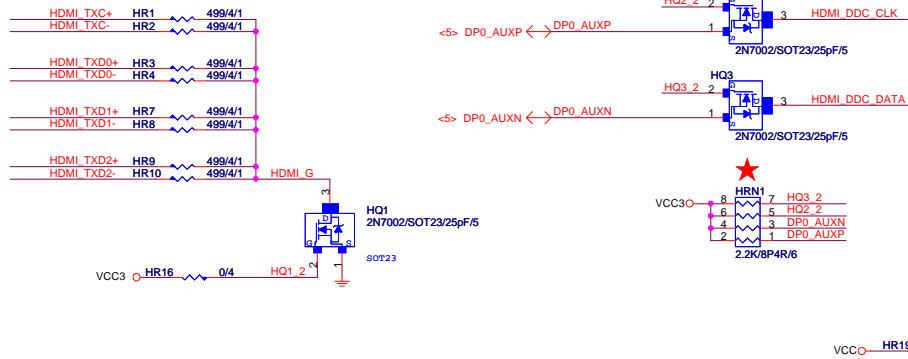
of

37





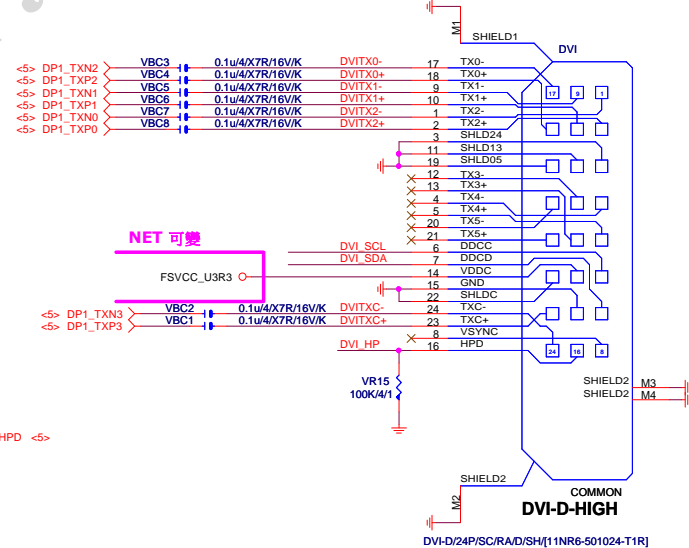
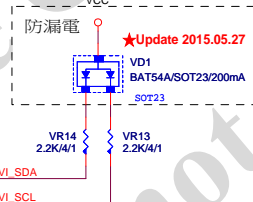
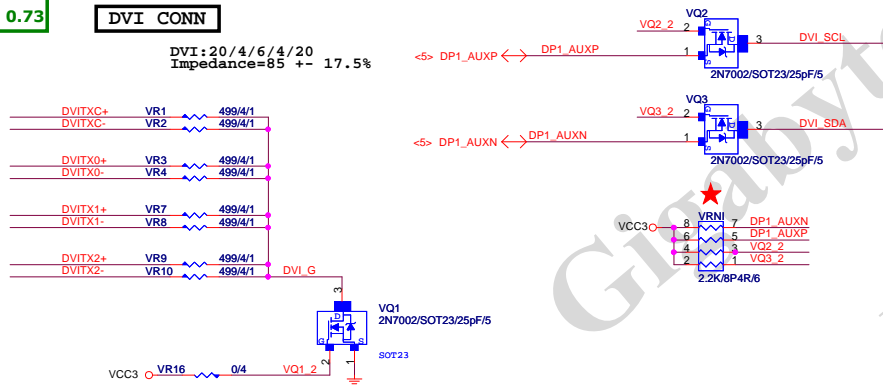




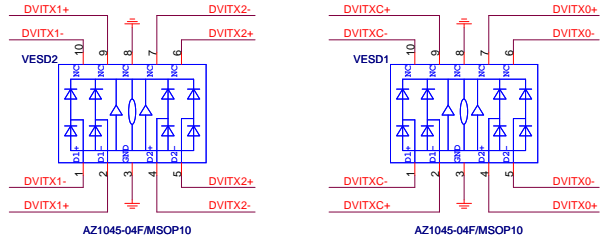
Rev: 0.73

DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%



Close to connector



NET 可變

Close to connector

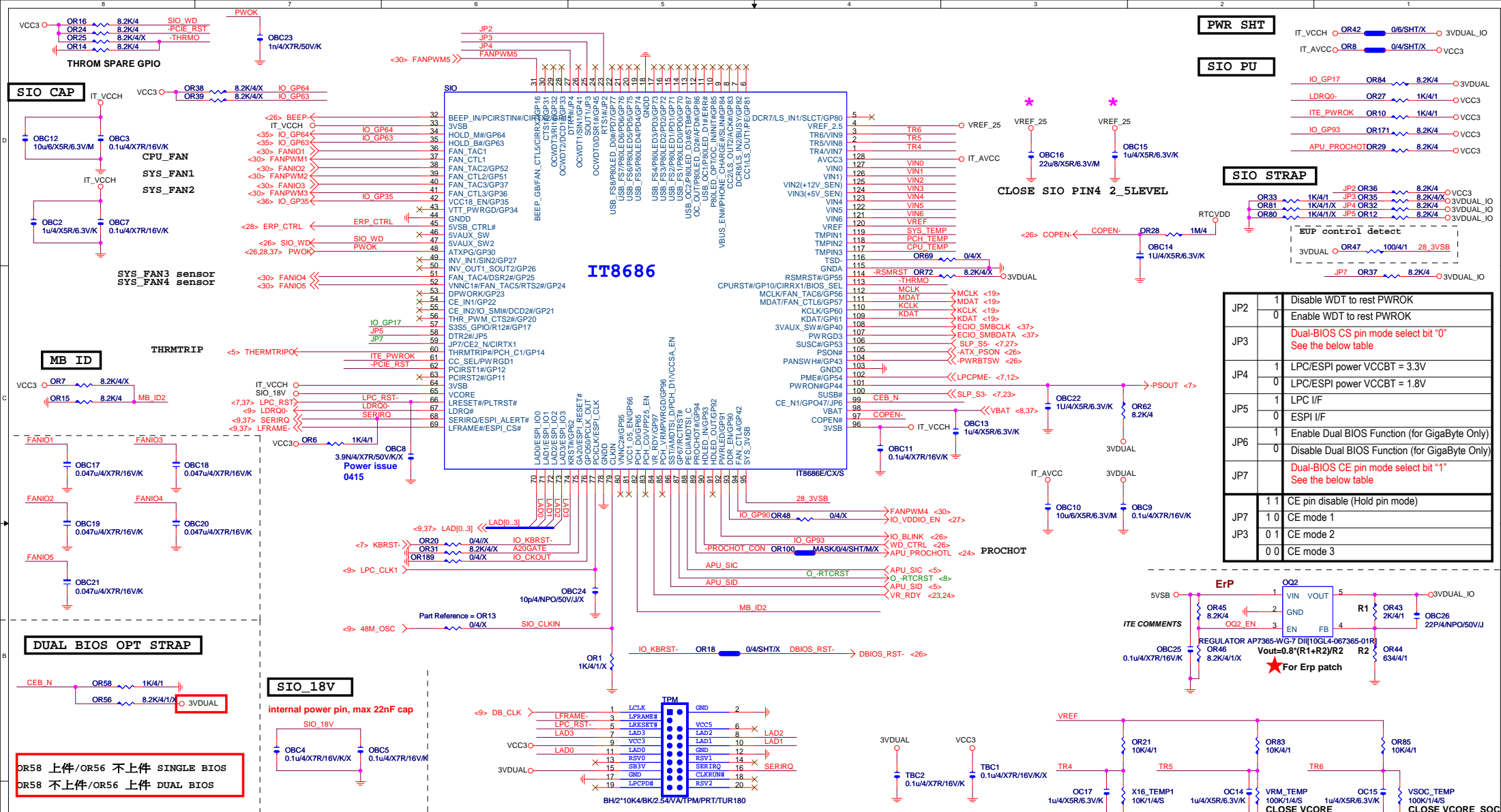


平躺式 DVI-D



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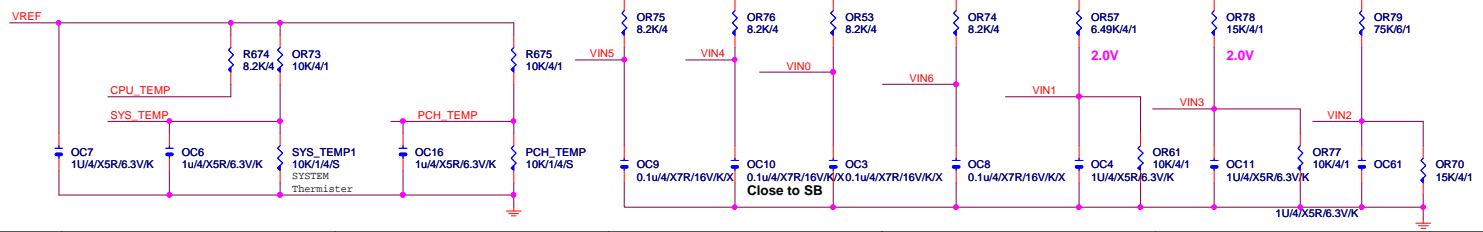
Title		
HDMI , DVI		
Size	Document Number	Rev
Custom	AB350-GAMING 3	1.01
Date:	Thursday, January 19, 2017	Sheet 17 of 37



OR58 上件/OR56 不上件 SINGLE BIOS
OR58 不上件/OR56 上件 DUAL BIOS

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN OR SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

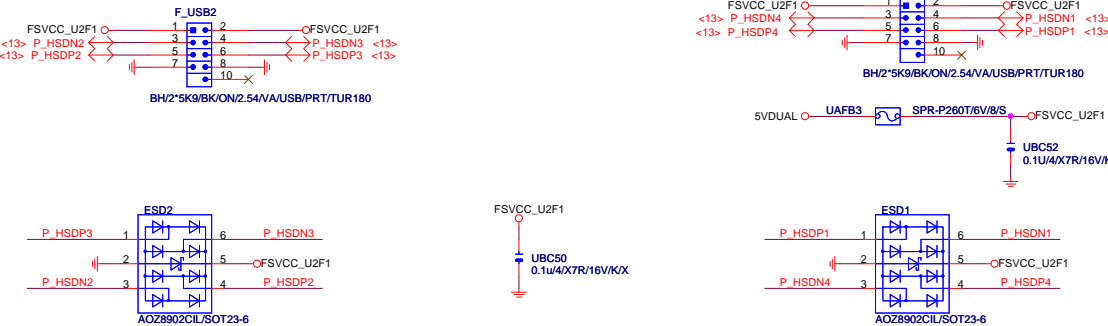
Hardware Monitor circuits



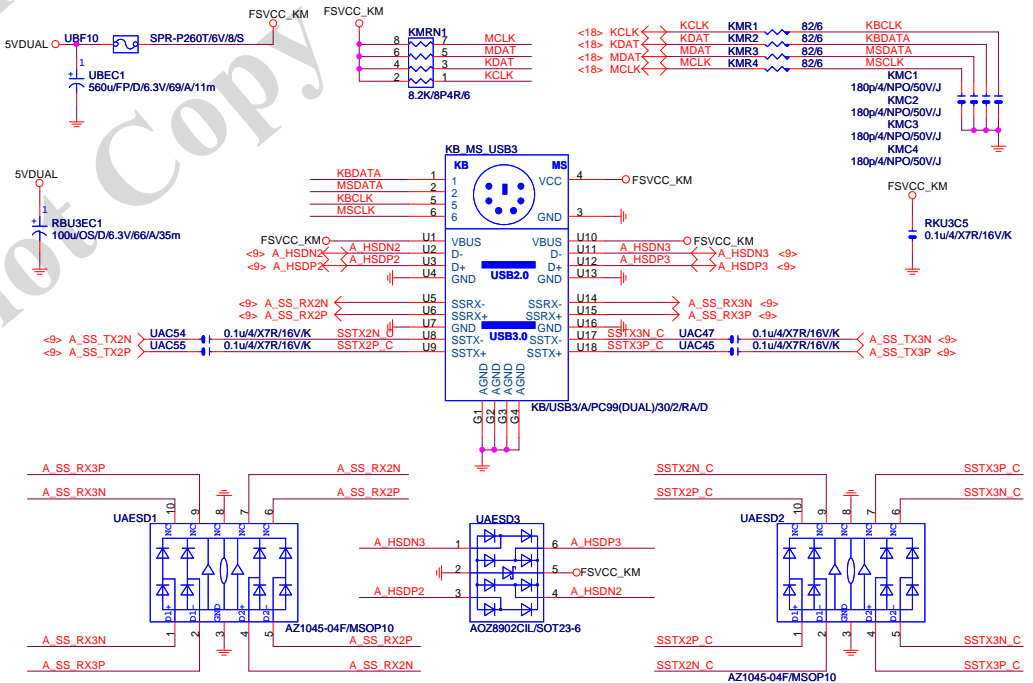
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ITE 8628CX , HWM , TPM , KB_MS_USB		
Size	Document Number	Rev
Custom	AB350-GAMING 3	1.01
Date: Thursday, January 19, 2017 Sheet 18 of 37		

FRONT SIDE USB2

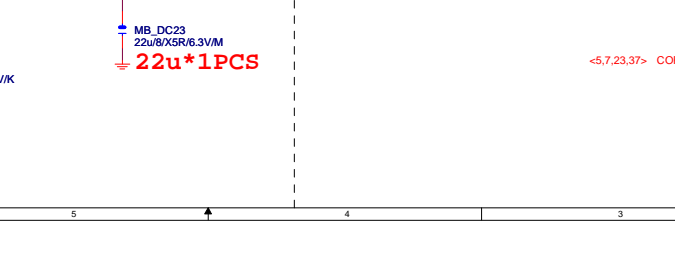
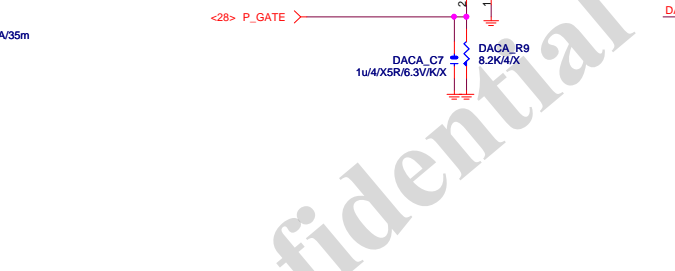
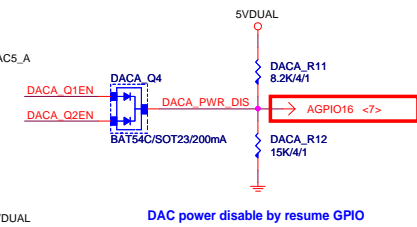
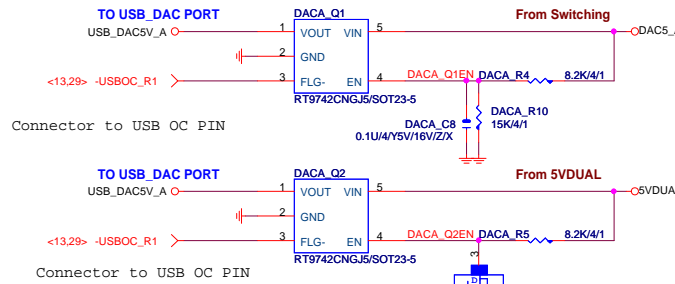
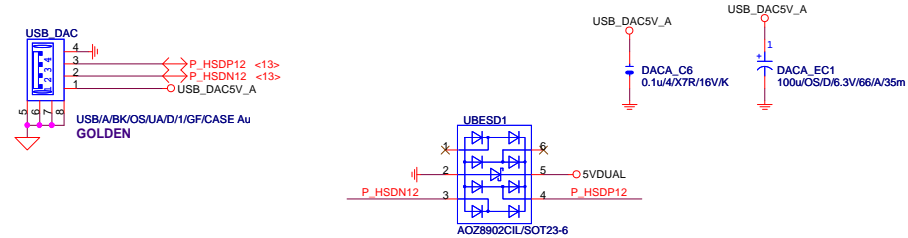
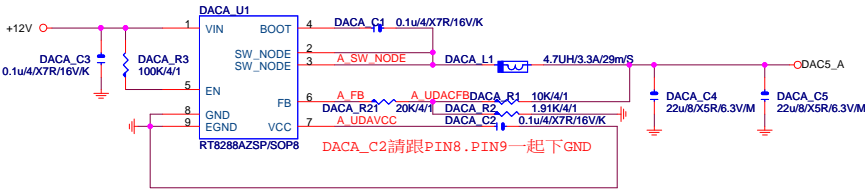


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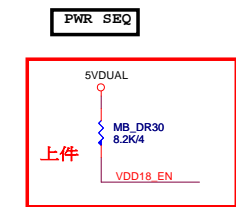
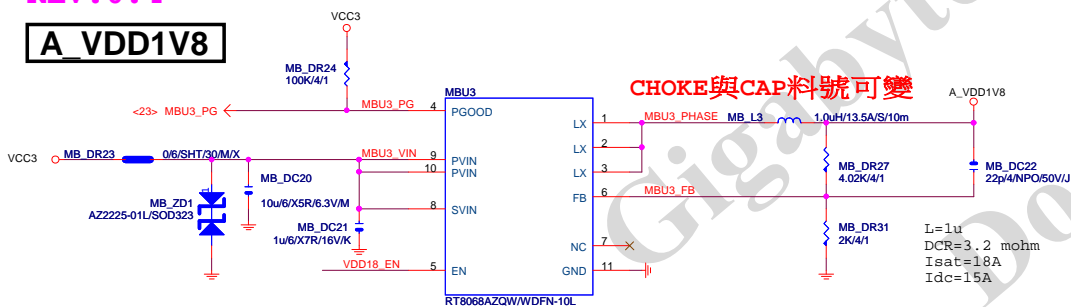
Title			
F_USB30_20 , R_USB30			
Size	Document Number	Rev	
Custom	AB350-GAMING 3	1.01	
Date:	Thursday, January 19, 2017	Sheet	19 of 37

USB_DAC_A REV:0.12



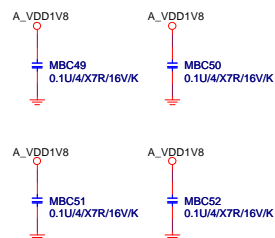
REV:0.4

A_VDD1V8



VPP CAP

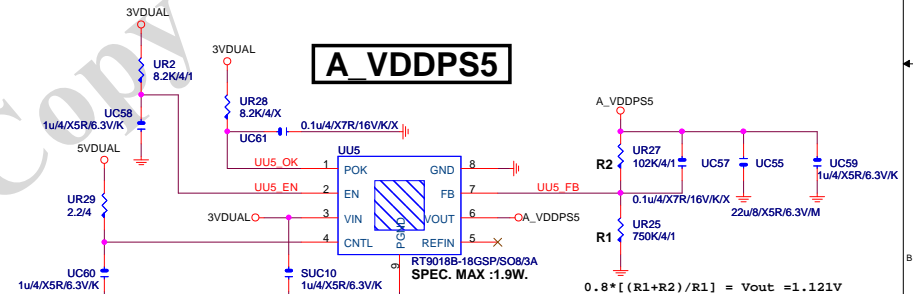
* 大電容 ≈0
22u*1PCS



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

<5,7,23,37> CORETYPE1 UR30 8.2K/4/1

A_VDDPS5



【技術通報R&D技術通報156】
RT9018 (RICHTEK) 與NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為100K以上電阻值

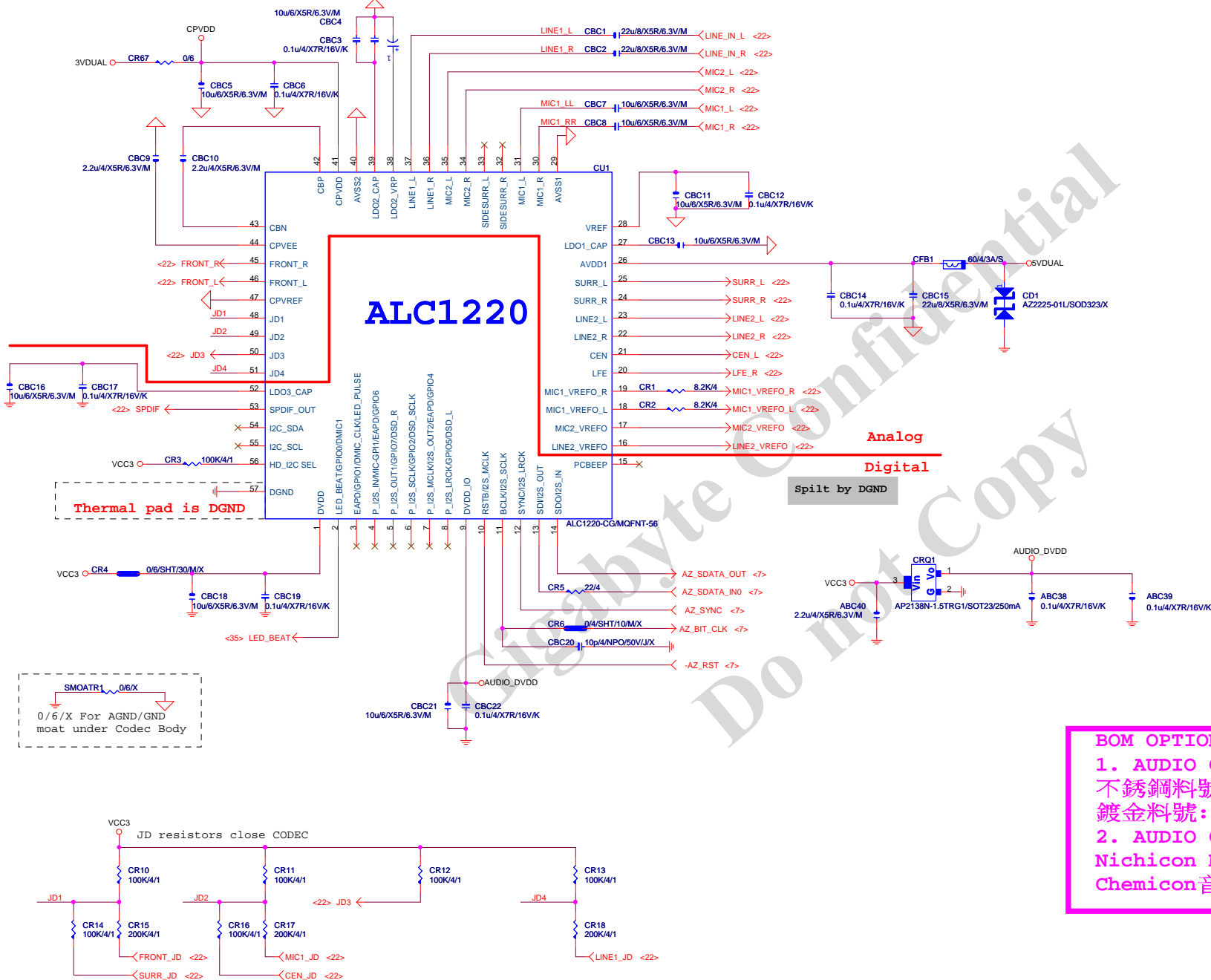
GIGABYTE

Title A_VDD1V8 , A_VDDPS5		
Size Custom	Document Number AB350-GAMING 3	Rev 1.01
Date Monday, January 16, 2017	Sheet 20	of 37

Rev 0.5

ALC1220 5H+1S+NO AMP

CEC1
100uF/D/10V/6*5[11CE2-651000-05R 11CE2-651000-12R]

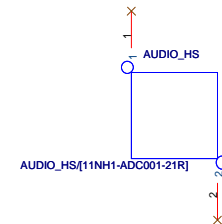


LAYOUT注意:螺絲孔下AGND方式
1. MH1,MH2全部下AGND

MH1 AGND MH2 AGND

LAYOUT注意:是否要加?
AGND切割線

音效區域印刷



BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A2R

鍍金料號:11NR6-403025-92R

2. AUDIO CAP

Nichicon MW音效電容 : 11CE1-651000-12R

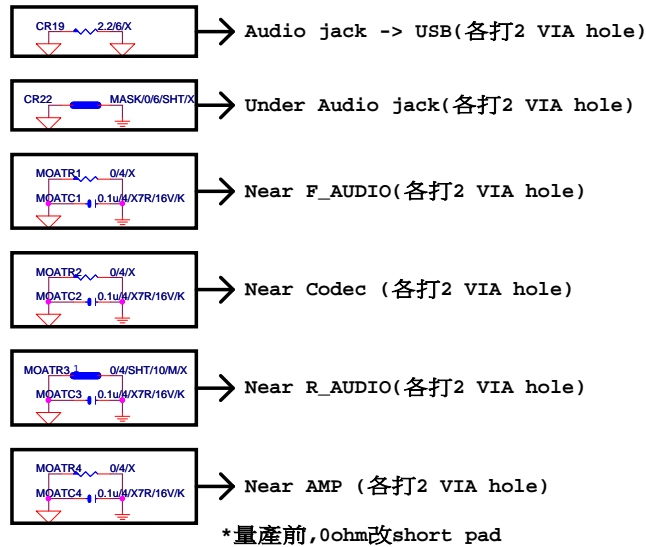
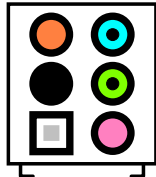
Chemicon音效電容 : 11CE2-651000-05R

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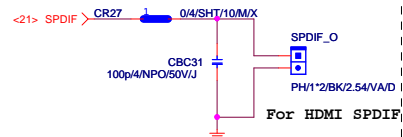
Title	ALC1220 CODEC	
Size	Document Number	Rev
Custom	AB350-GAMING 3	1.01
Date:	Thursday, January 19, 2017	Sheet 21 of 37

Rev 0.5

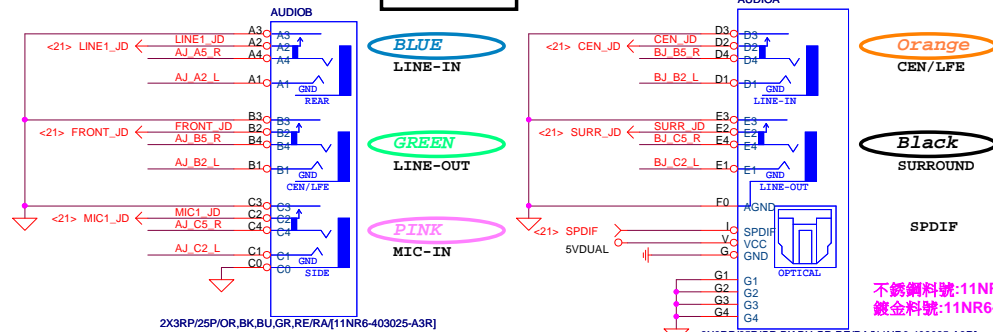
AZALIA JACK



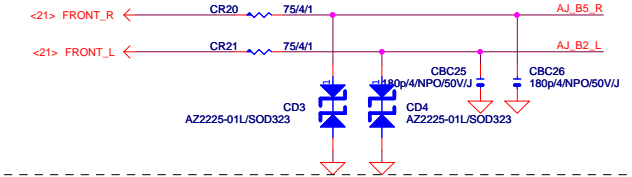
SPDIF_OUT



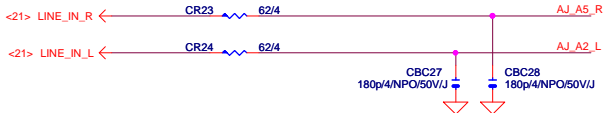
AZALIA JACK



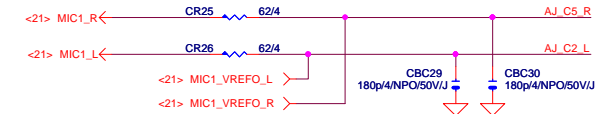
LINE-OUT



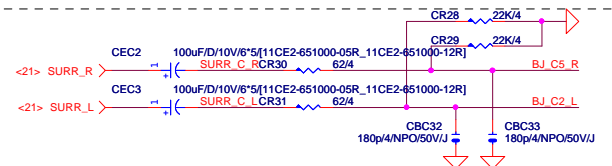
LINE-IN



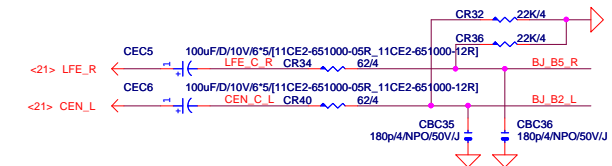
MIC-IN



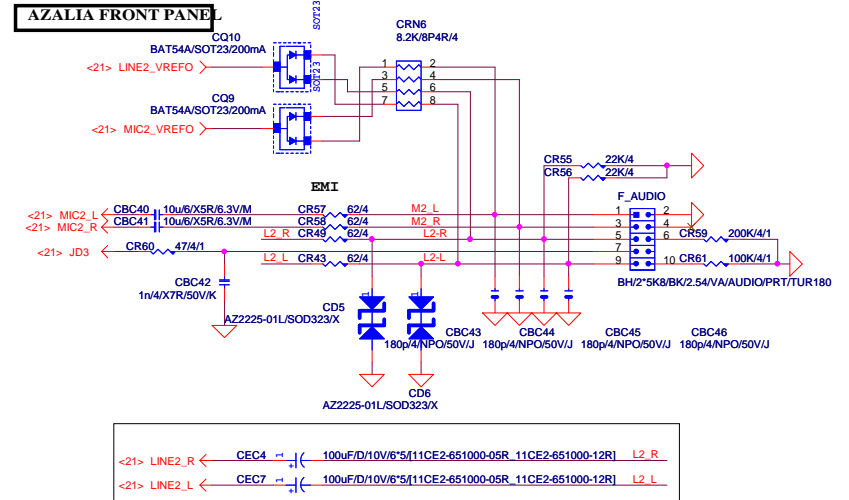
SURROUND



CEN/LFE

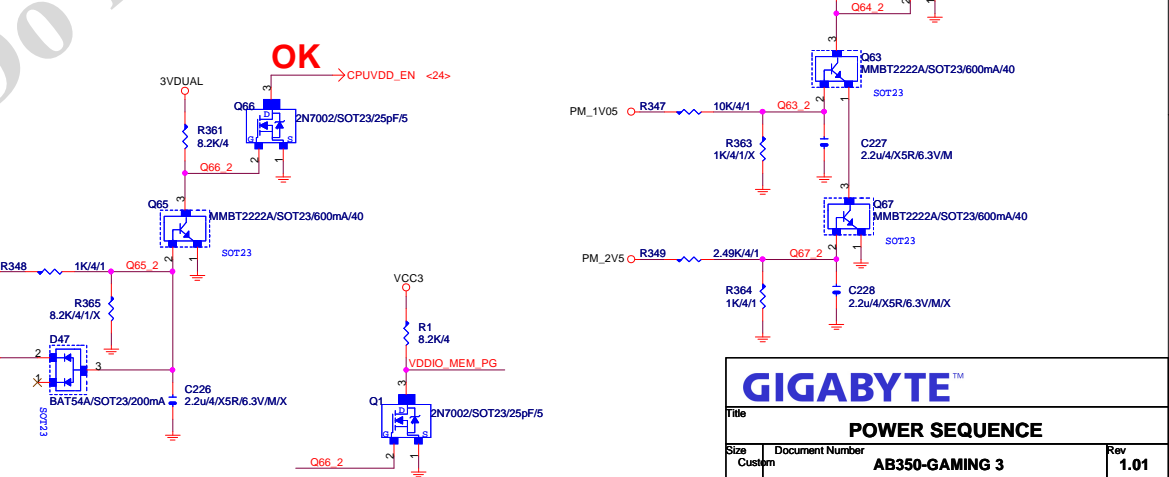
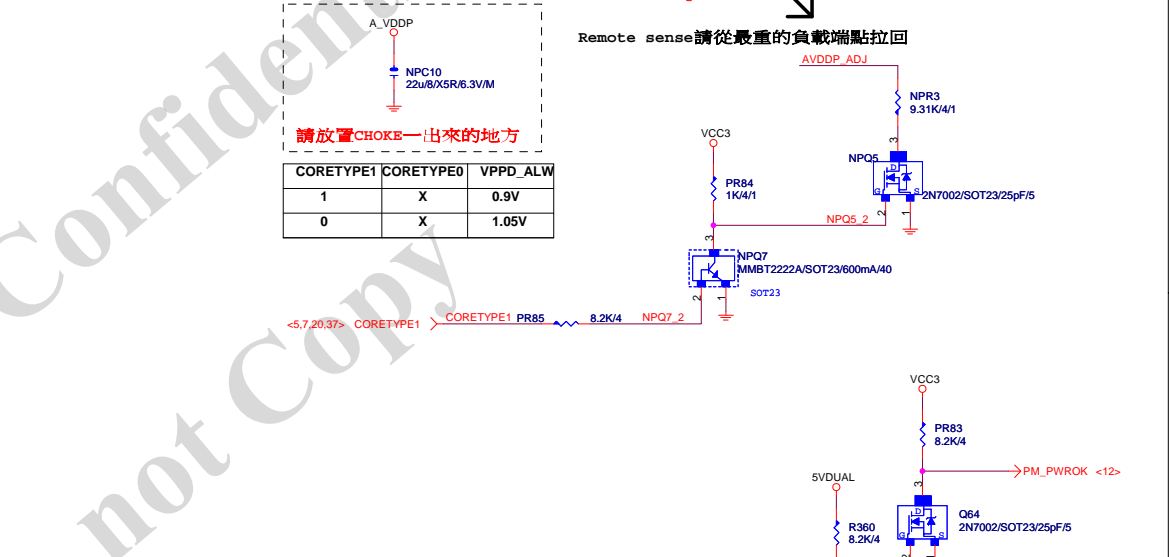
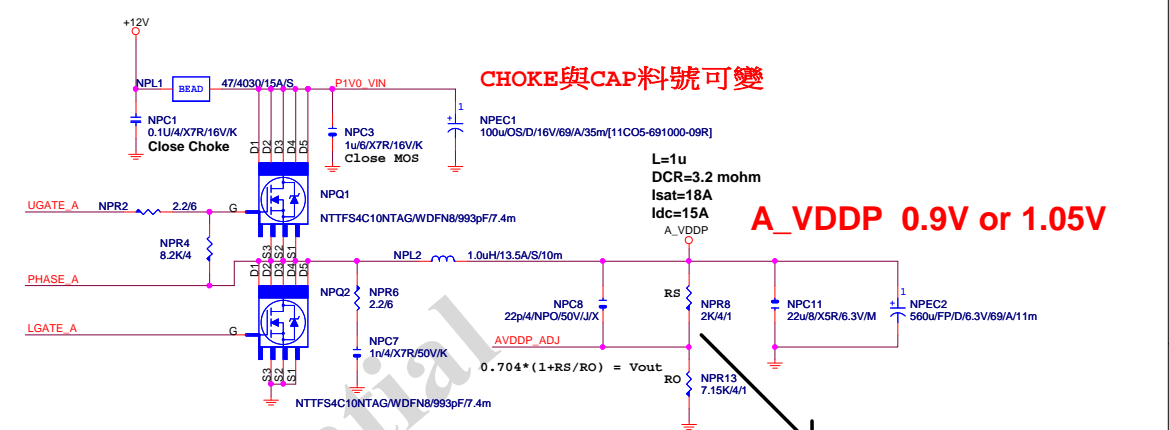
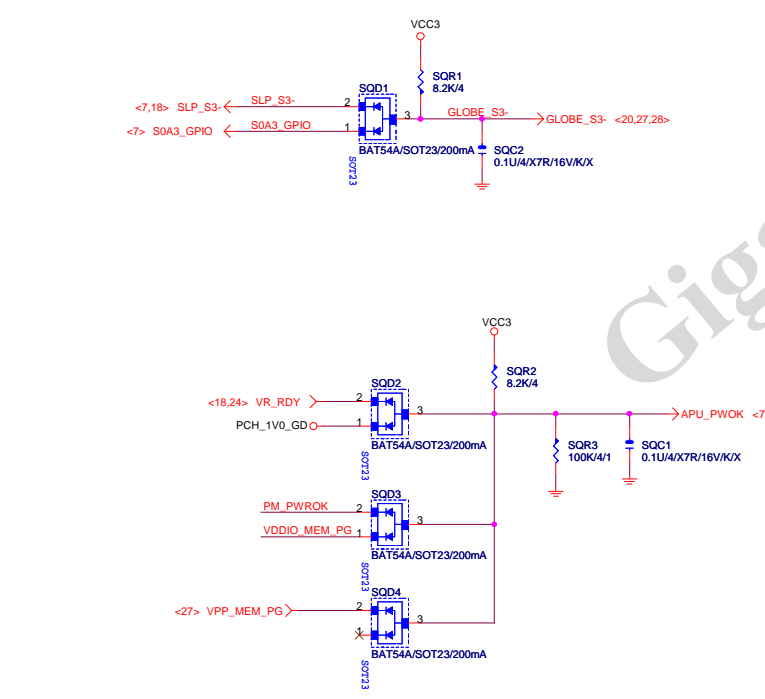
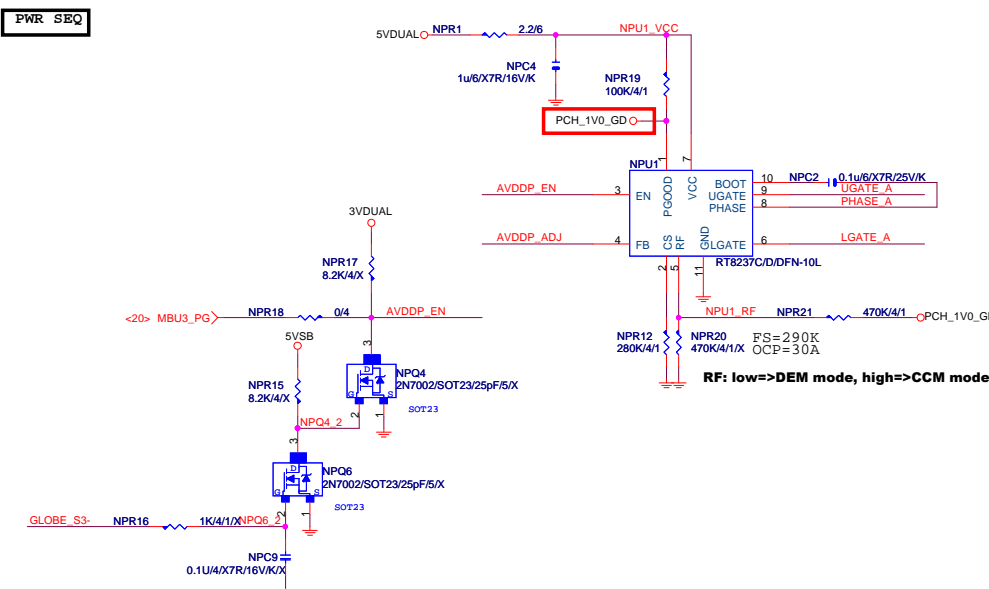


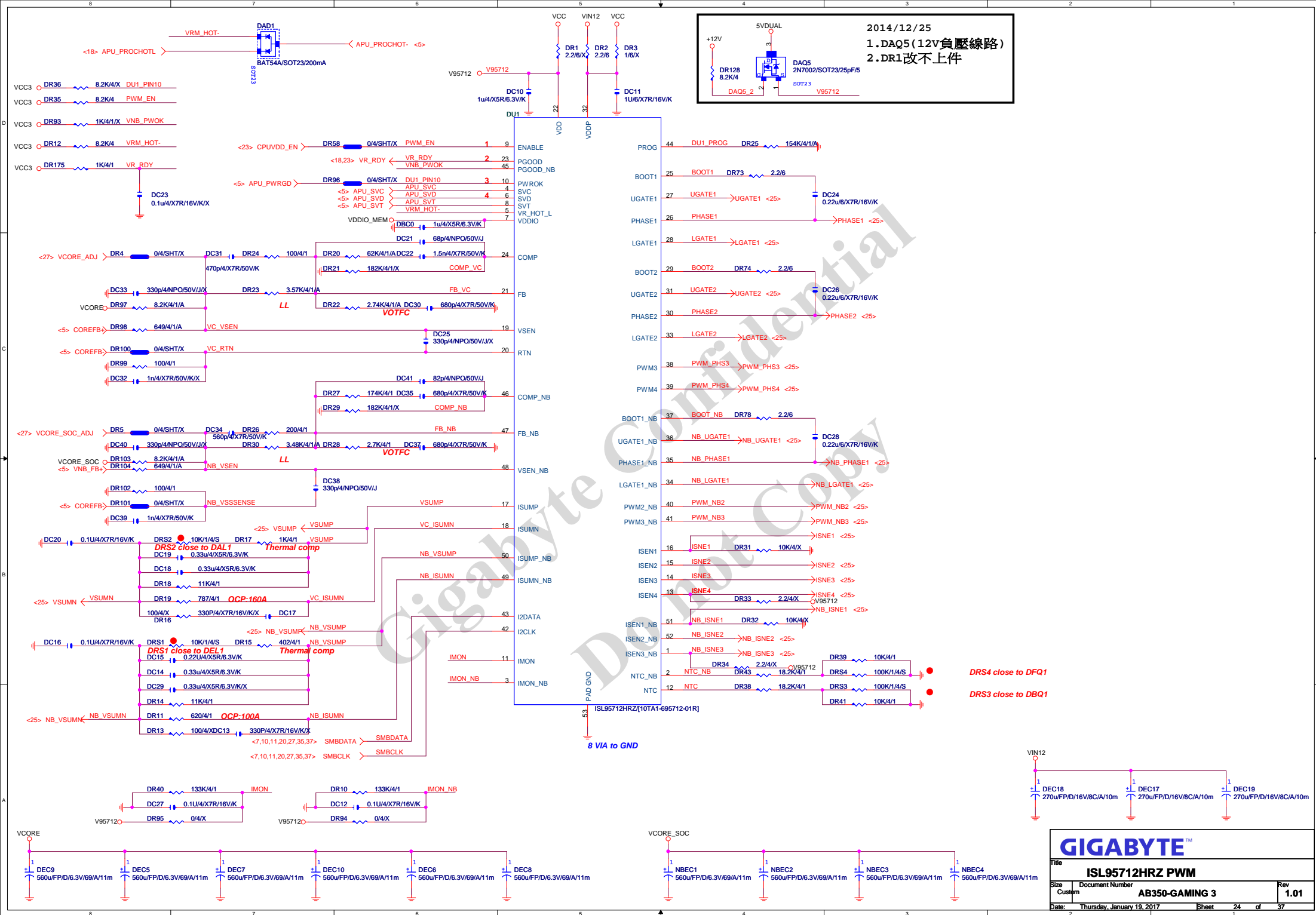
AZALIA FRONT PANEL

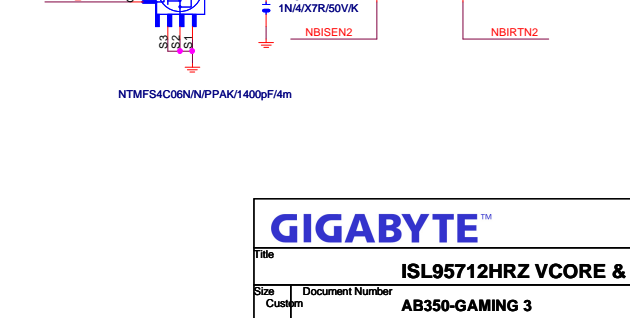
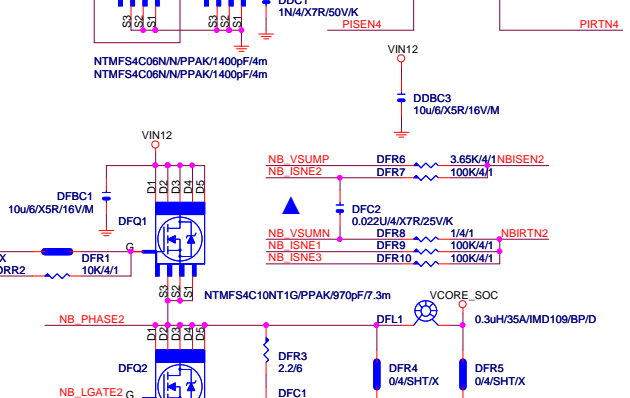
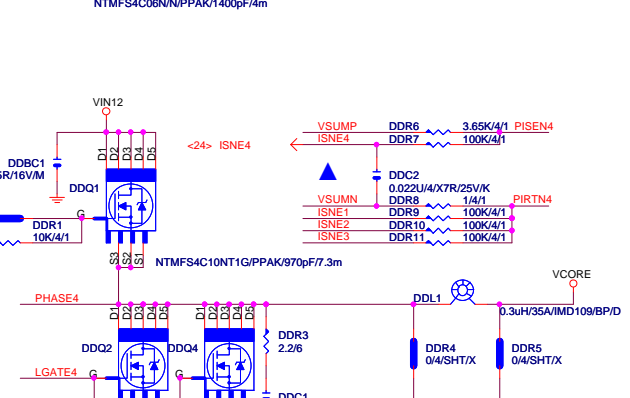
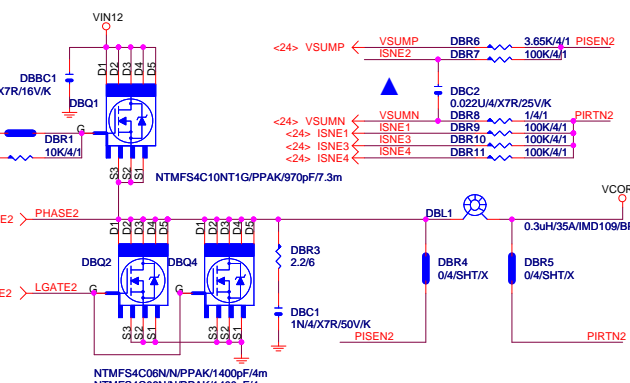
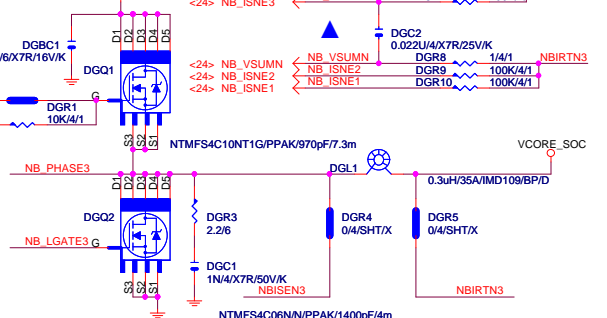
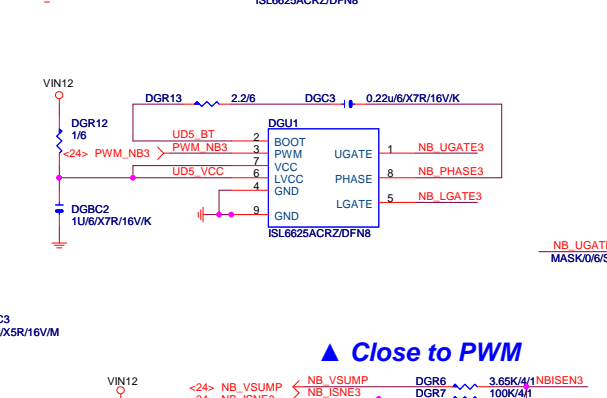
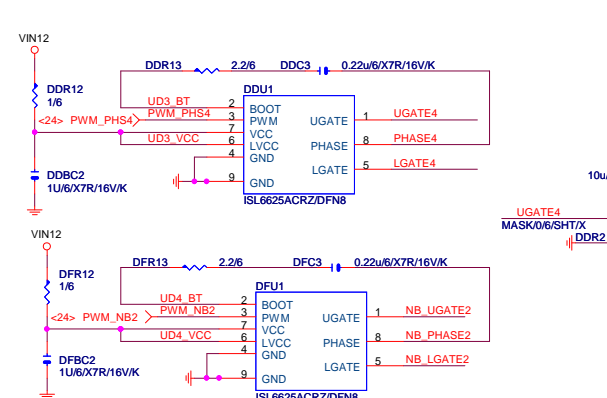
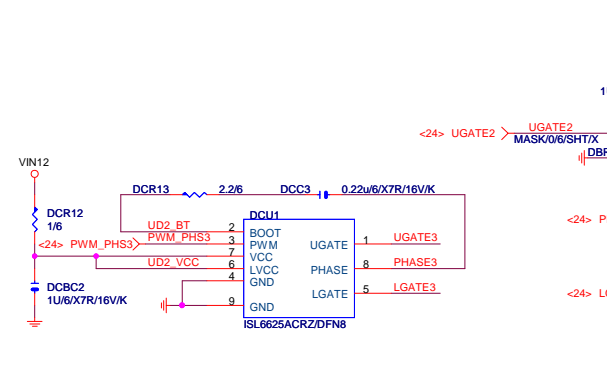
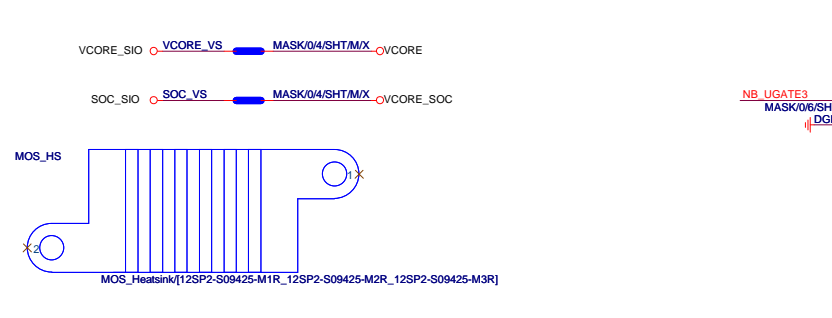
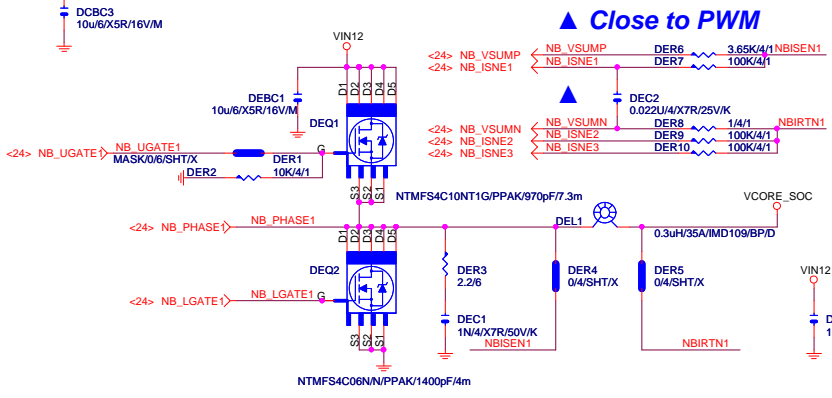
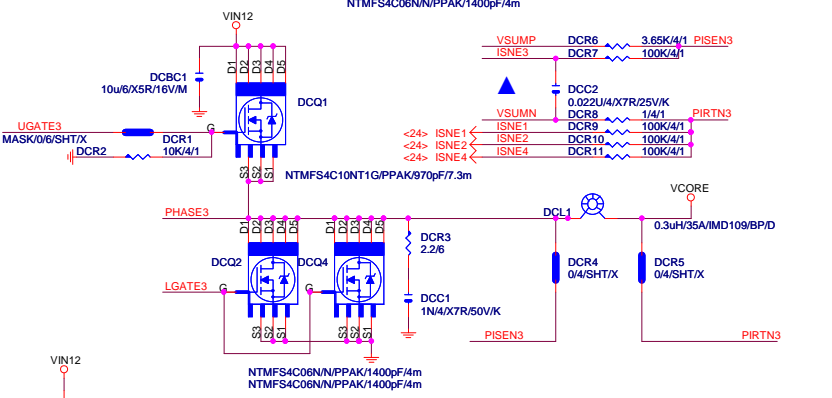
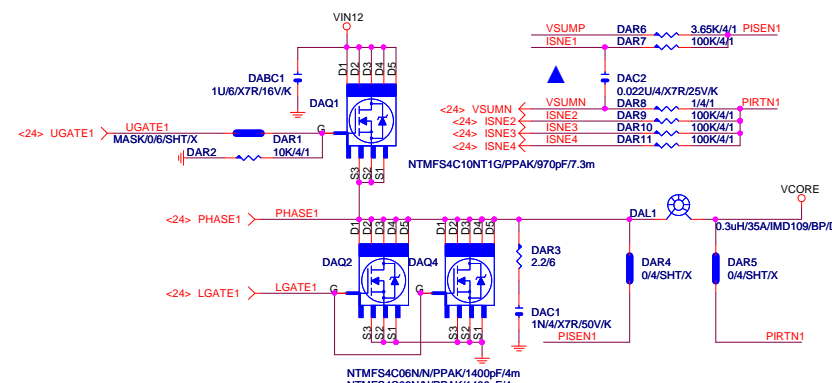


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Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	AB350-GAMING 3	1.01
Date:	Thursday, January 19, 2017	Sheet 22 of 37

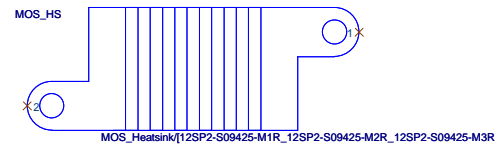


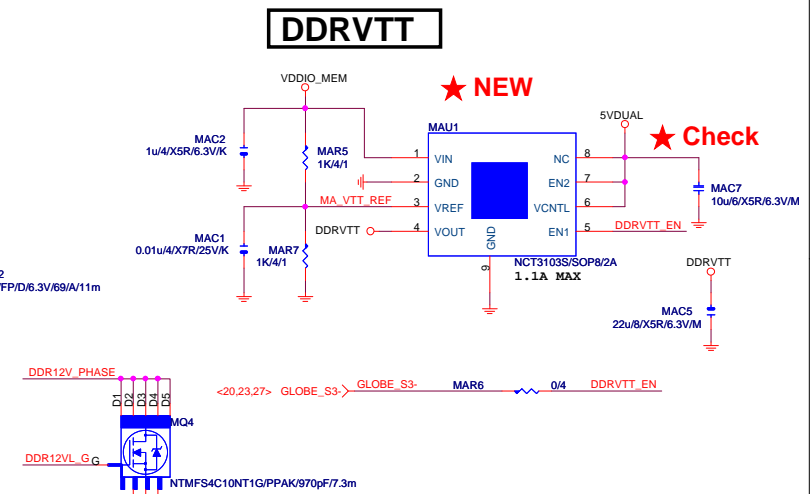
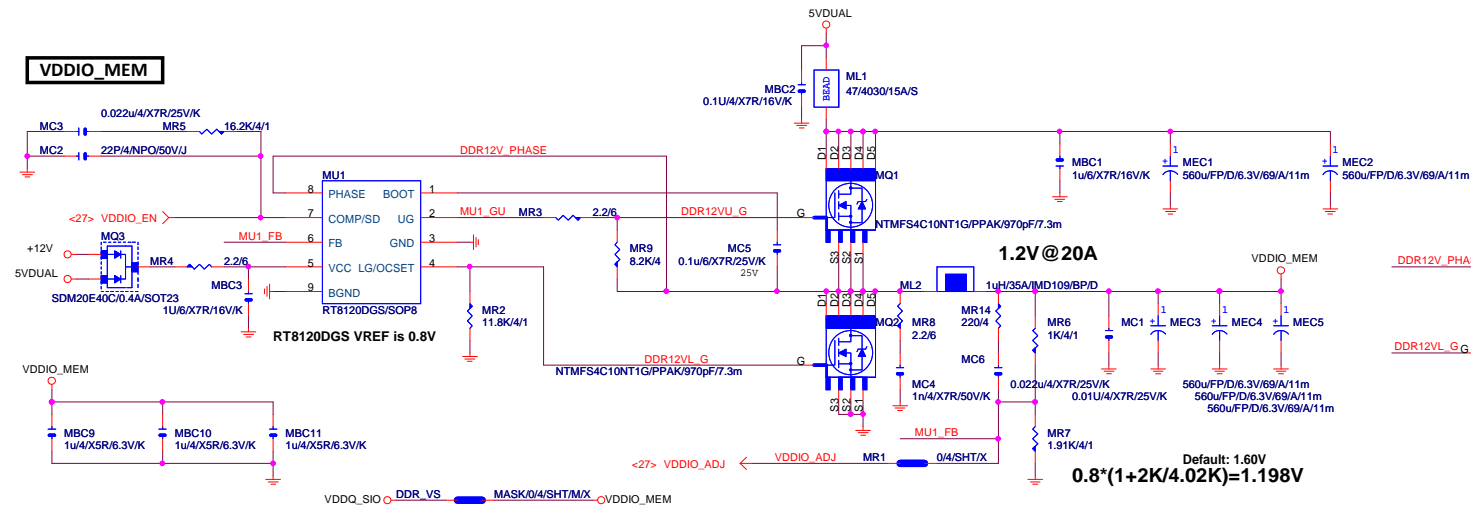
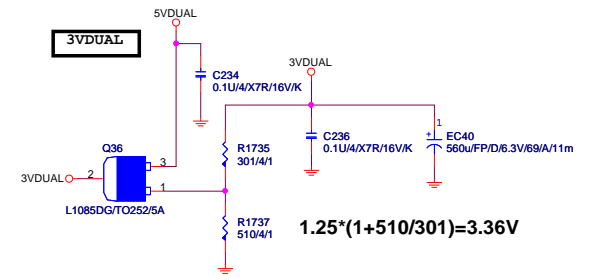
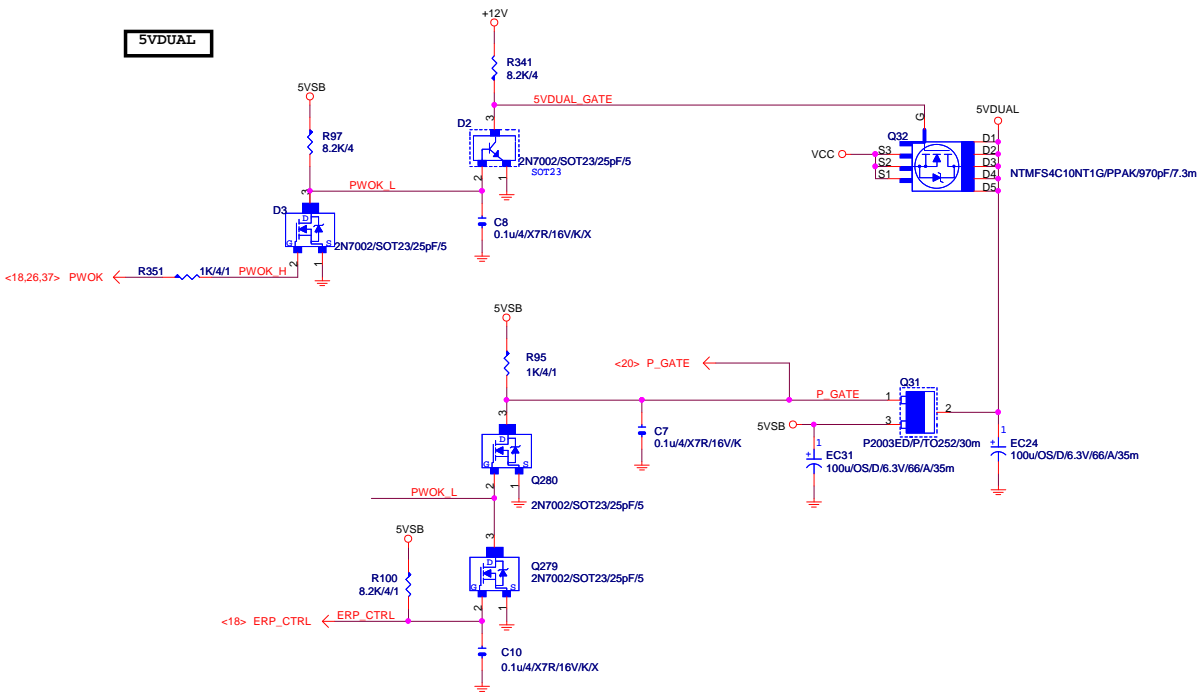




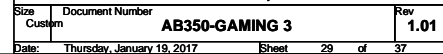
Close to PWM

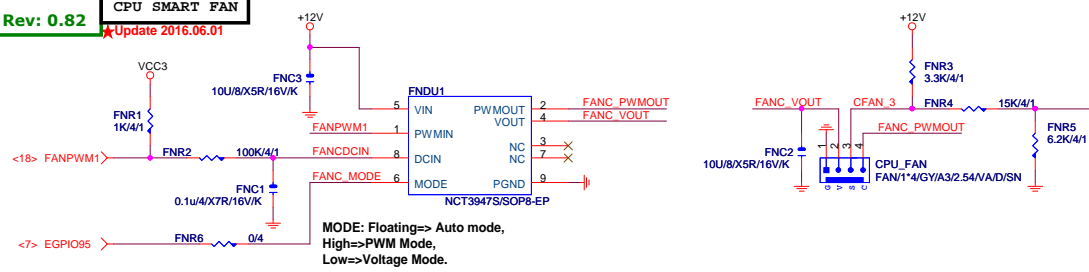
Close to PWM



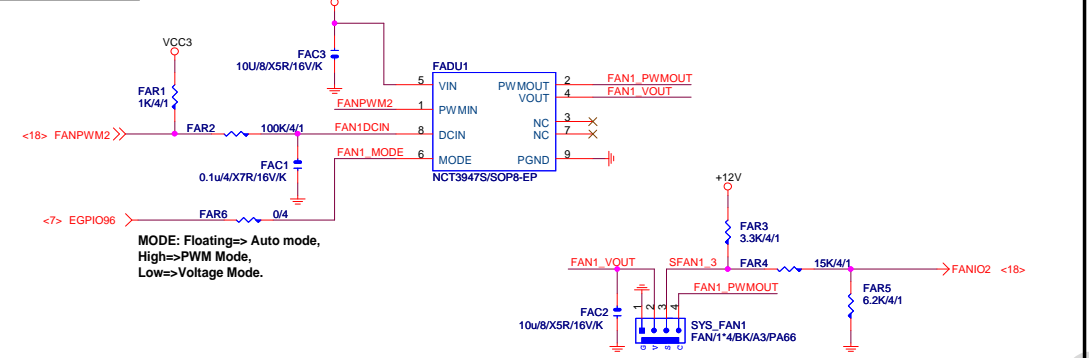


GIGABYTE™		
Title		
DDR PWR, 5VDUAL, ERP		
Size	Document Number	Rev
Custom	AB350-GAMING 3	1.01
Date:	Thursday, January 19, 2017	Sheet 28 of 37

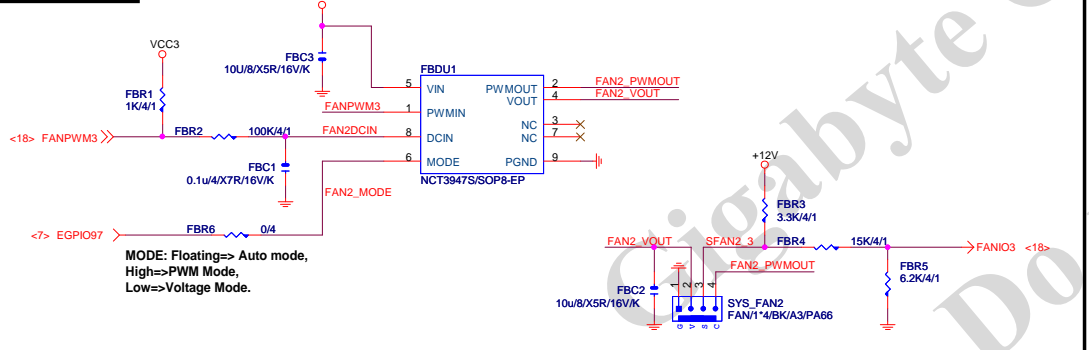




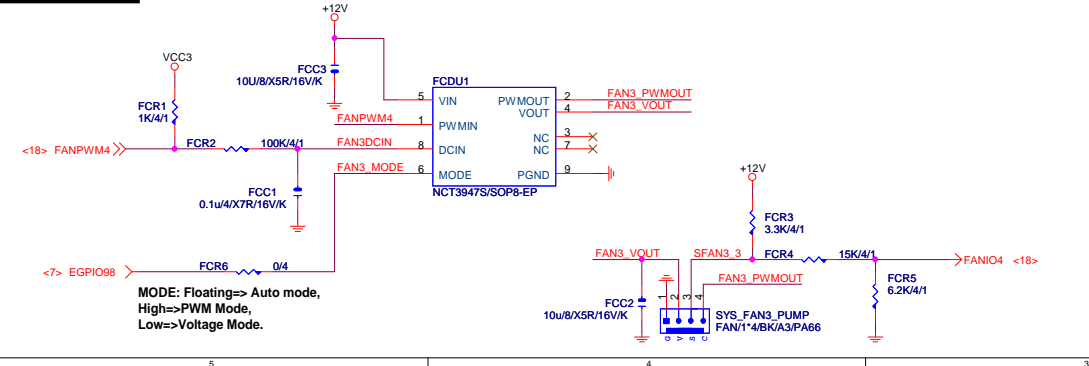
SYSTEM FAN1



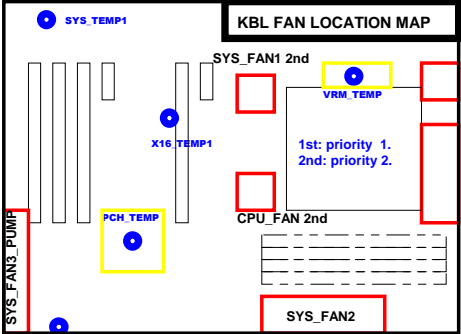
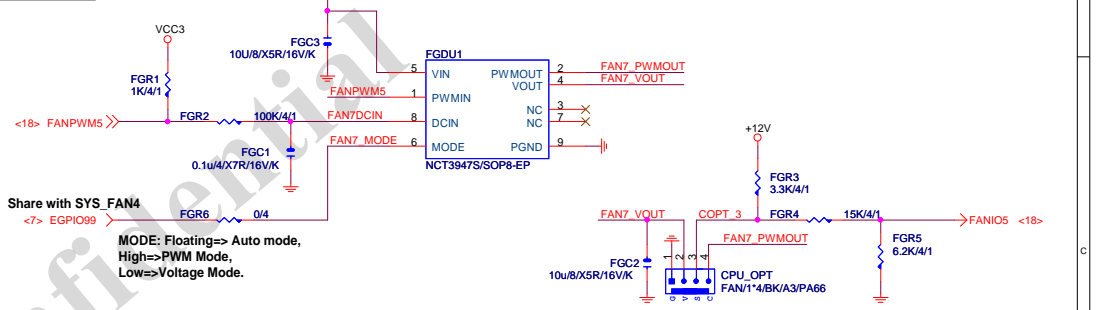
SYSTEM FAN2



SYSTEM FAN3



CPU_OPT



5 FAN from IO

TEMP SENSE

VRM_TEMP

1st: priority 1.
2nd: priority 2.

CPU_FAN 1st
OPT_FAN

AB350-GAMING 3

1.01

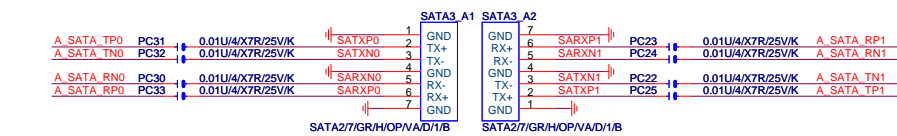
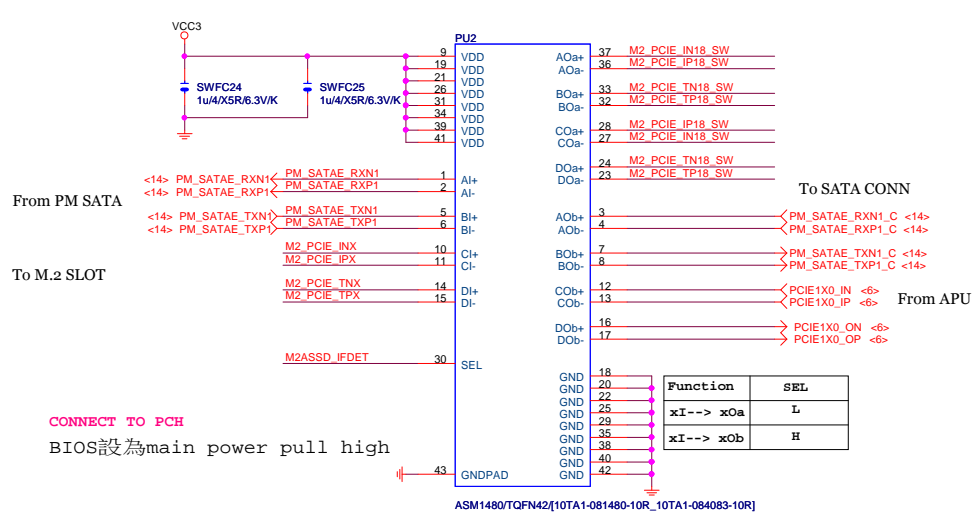
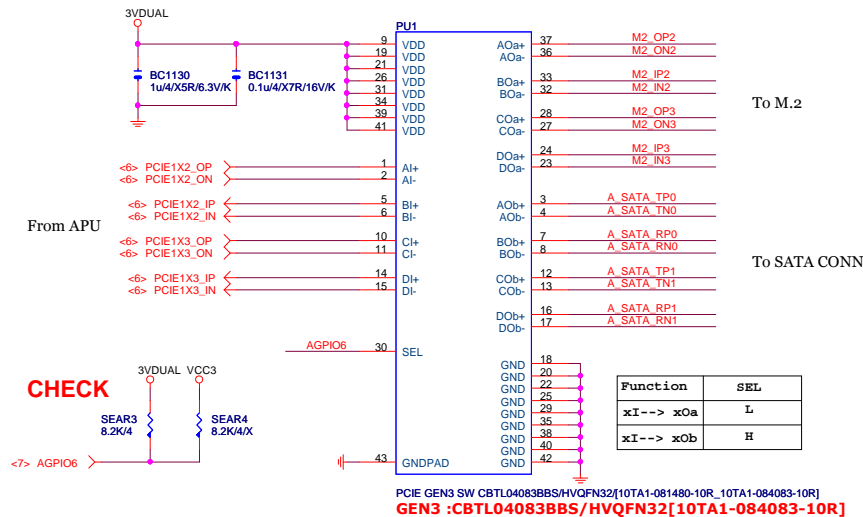
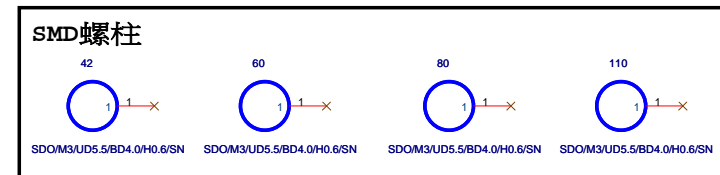
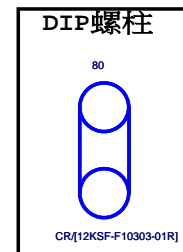
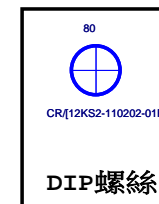
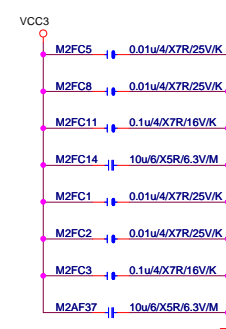
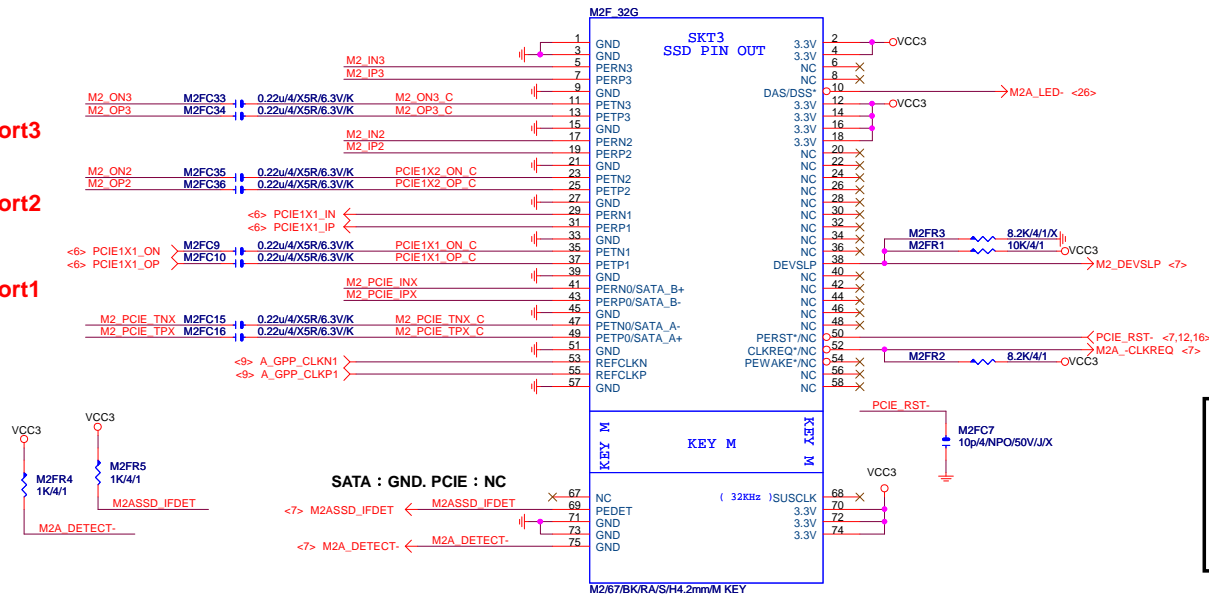
Rev 0.5

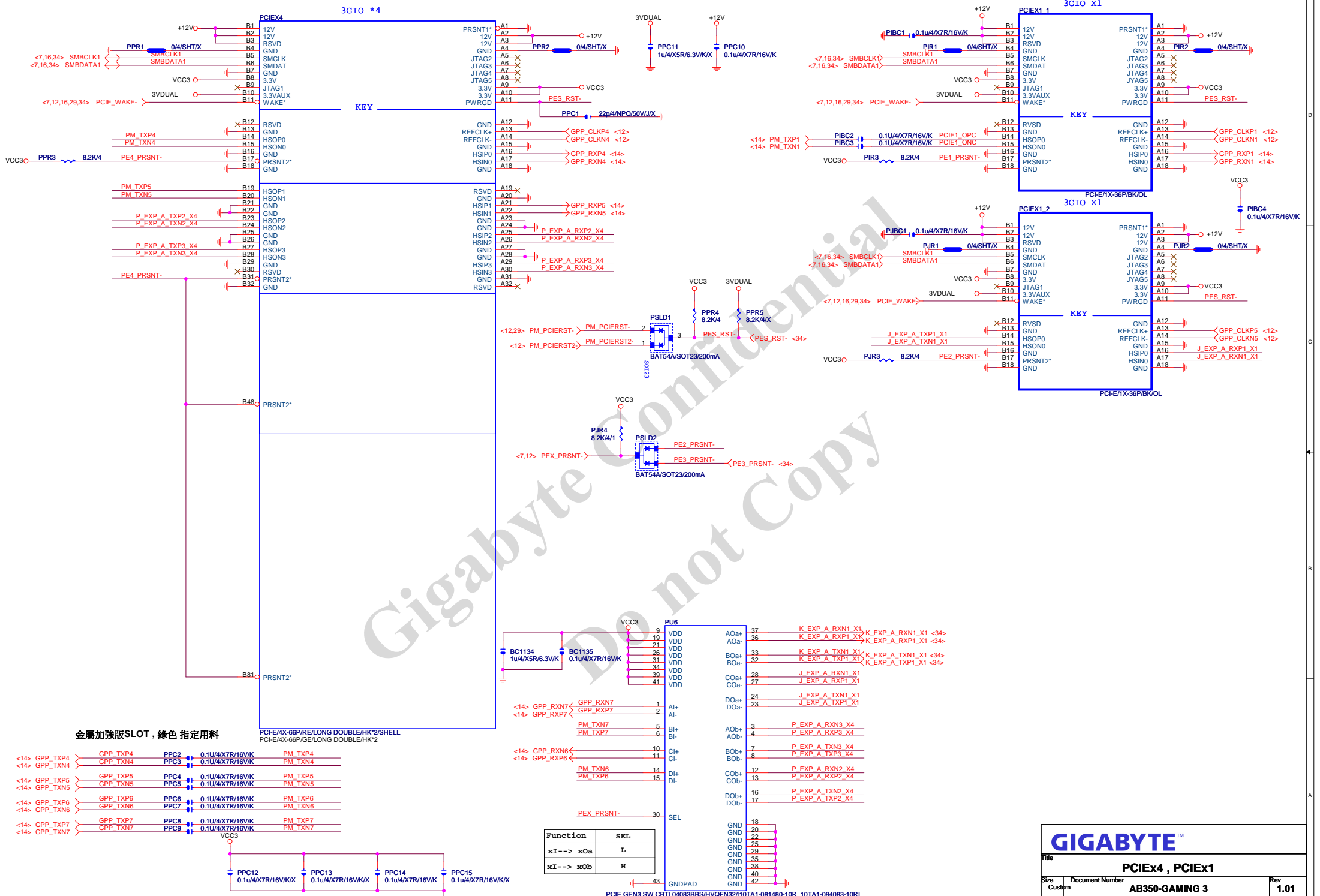
M.2 Lane4 from AM4 port3

M.2 Lane4 from AM4 port2

M.2 Lane4 from AM4 port1

by SWITCH Select





金屬加強版SLOT，綠色 指定用料

PCI-E/4X-66P/RE/LONG DOUBLE/HK*2/SHELL
PCI-E/4X-66P/GE/LONG DOUBLE/HK*2

<14> GPP_TXP4	GPP_TXP4	PPC2	0.1u/4X7R/16V/K	PM_TXP4
<14> GPP_TXN4	GPP_TXN4	PPC3	0.1u/4X7R/16V/K	PM_TXN4
<14> GPP_TXP5	GPP_TXP5	PPC4	0.1u/4X7R/16V/K	PM_TXP5
<14> GPP_TXN5	GPP_TXN5	PPC5	0.1u/4X7R/16V/K	PM_TXN5
<14> GPP_TXP6	GPP_TXP6	PPC6	0.1u/4X7R/16V/K	PM_TXP6
<14> GPP_TXN6	GPP_TXN6	PPC7	0.1u/4X7R/16V/K	PM_TXN6
<14> GPP_TXP7	GPP_TXP7	PPC8	0.1u/4X7R/16V/K	PM_TXP7
<14> GPP_TXN7	GPP_TXN7	PPC9	0.1u/4X7R/16V/K	PM_TXN7

Function	SEL
xI--> x0a	L
xI--> x0b	H

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Title

PCIEx4 , PCIeX1

Size

Custom

Document Number

AB350-GAMING 3

Rev

1.01

Date

Thursday, January 19, 2017

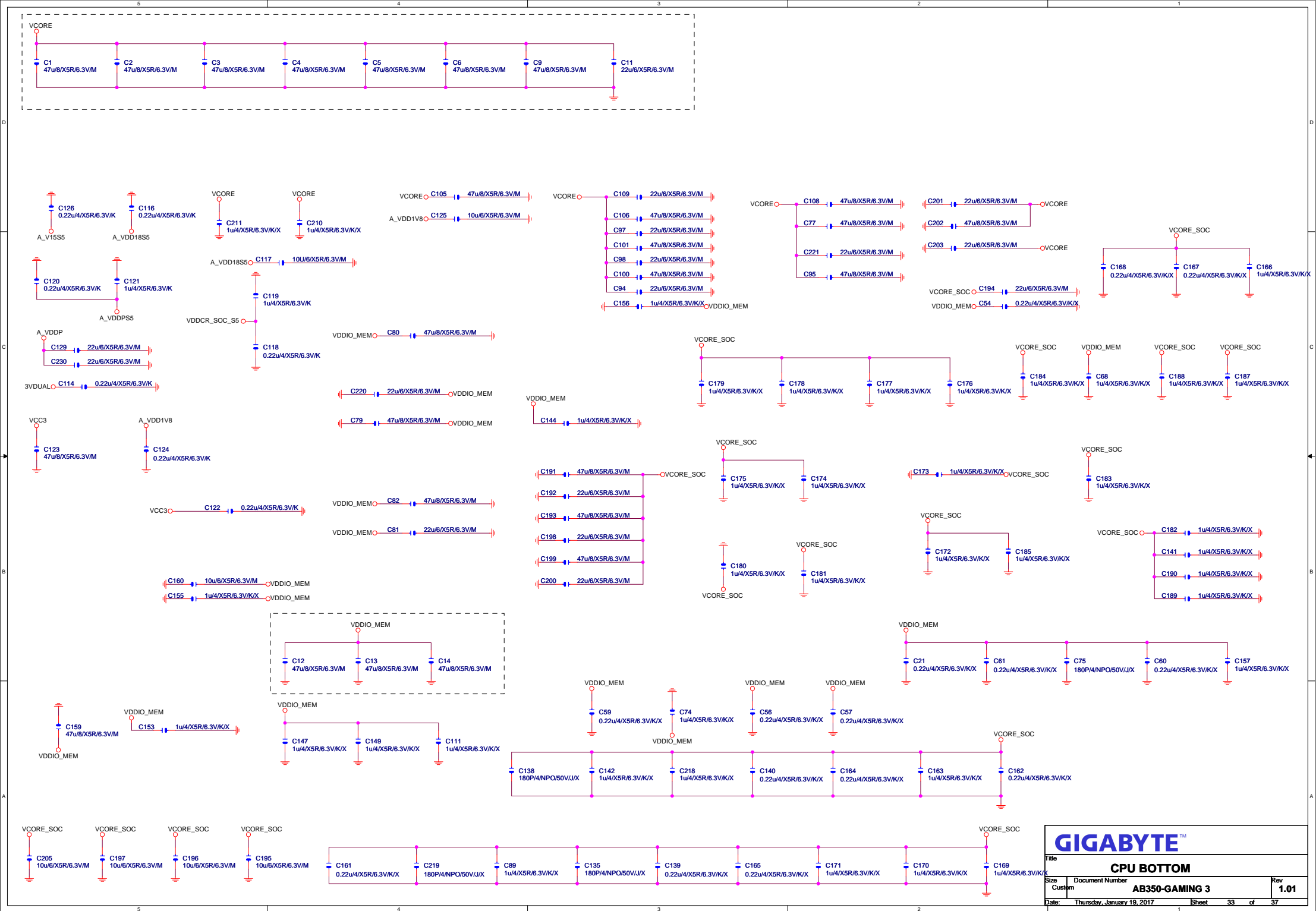
Sheet

32

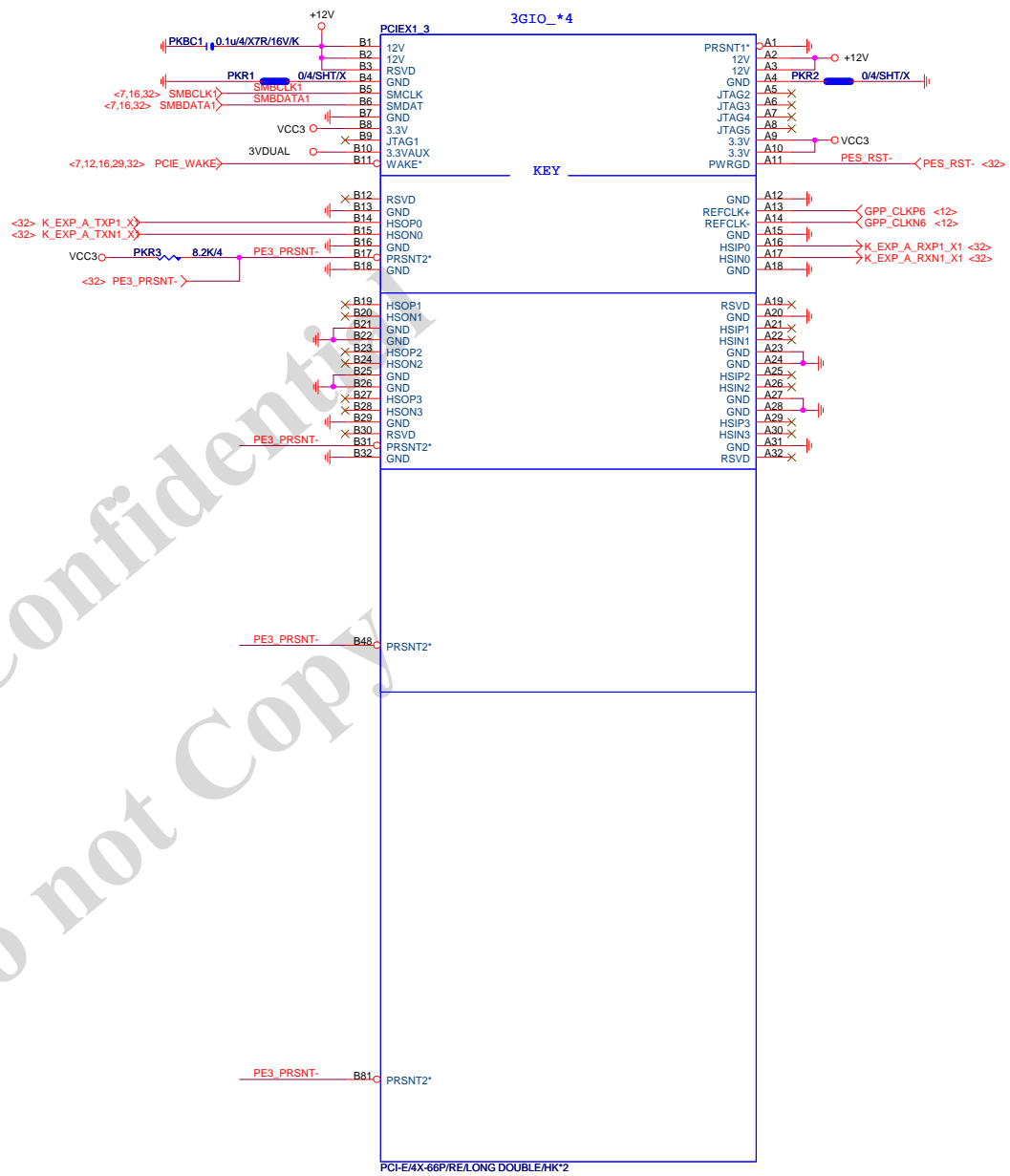
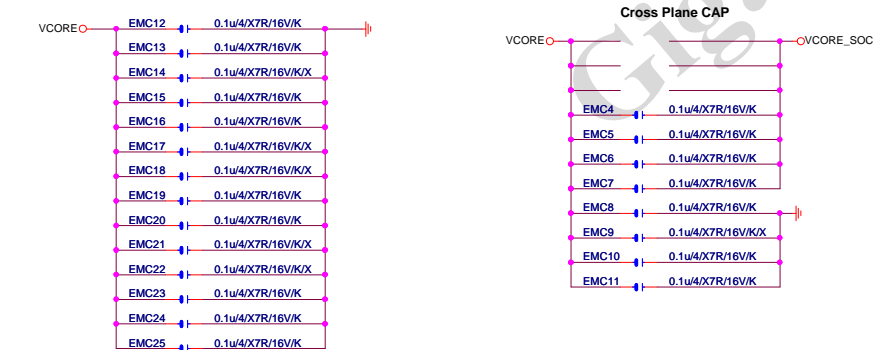
of

37

PCIe GEN3 SW CB TL04083BBS/HV/QFN32[10TA1-081480-10R_10TA1-084083-10R]



CPU TOP CAVITY

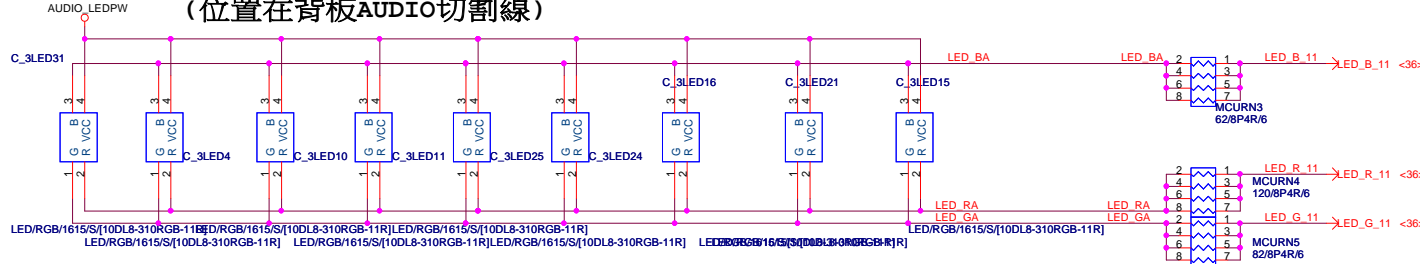


GIGABYTE™			
Title			
CPU TOP			
Size	Document Number		Rev
Custom	AB350-GAMING 3		1.01
Date:	Thursday, January 19, 2017	Sheet	34 of 37

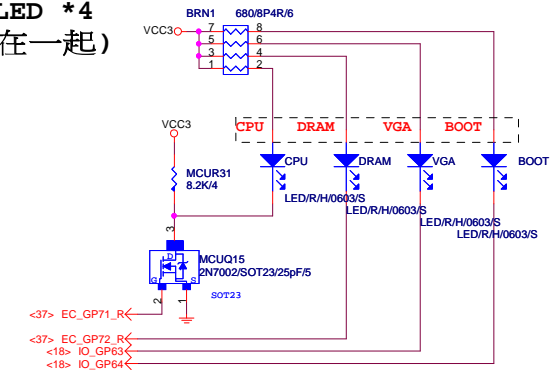
第一區 LED

Rev 0.63

FOR AUDIO 正發光 LED*40
(位置在背板AUDIO切割線)



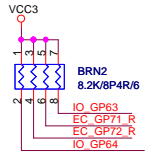
DEBUG PORT LED *4
(位置需擺放在一起)



用文字面表示

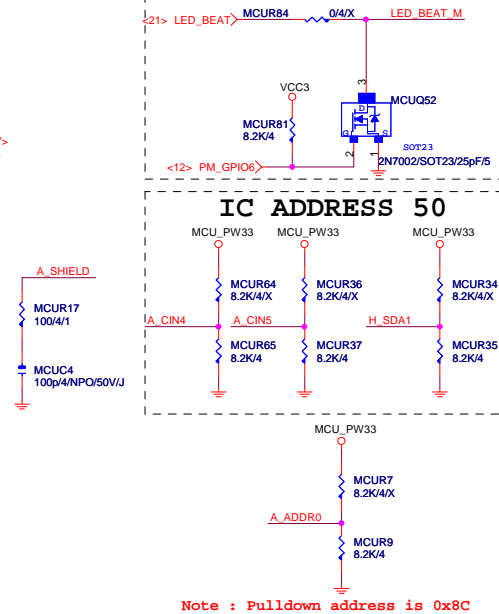
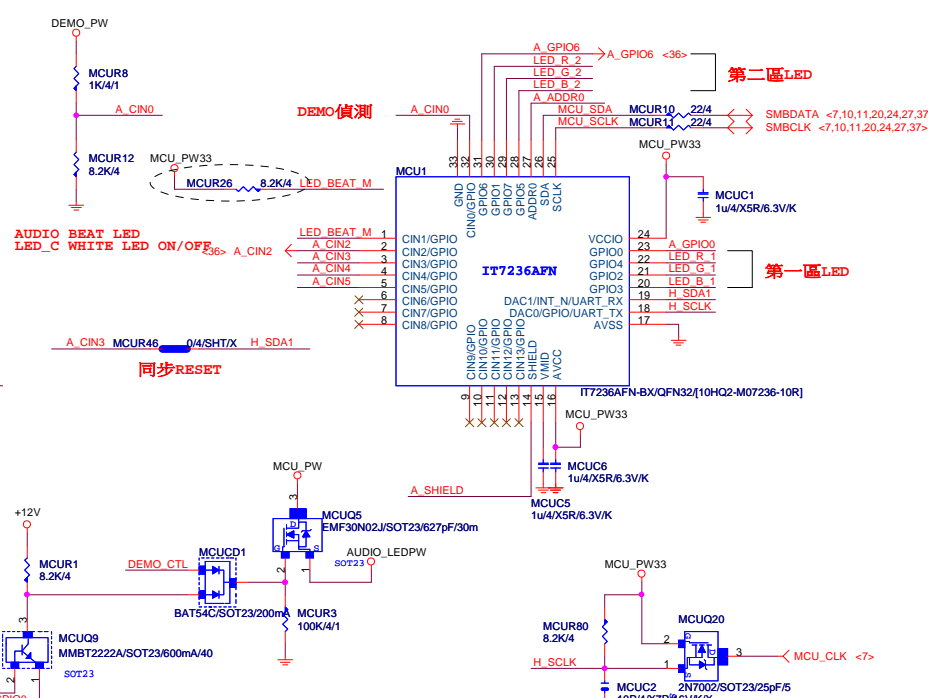
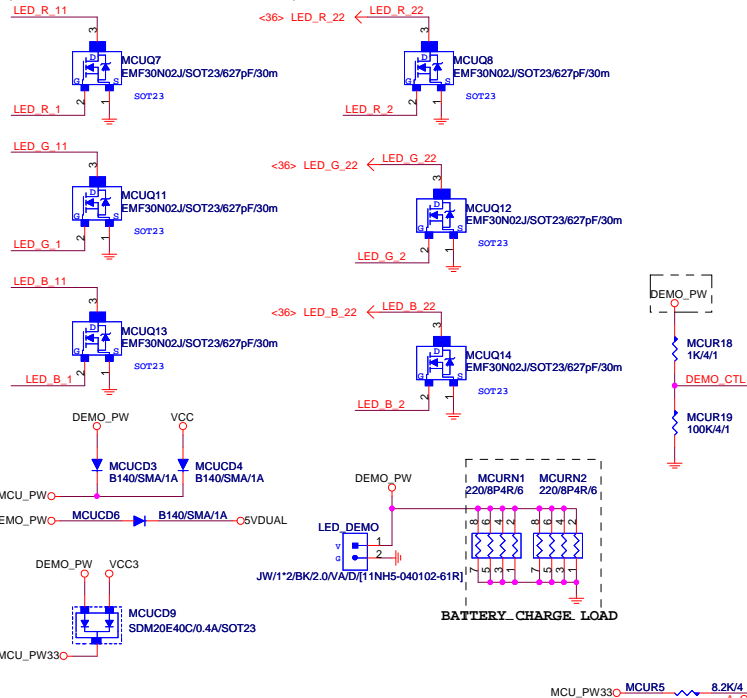
LED GPIO PIN DEFINE

EC_GP71_R	CPU DEBUG
EC_GP72_R	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEBUG
PM_GPIO5	LED_C LED SWITCH



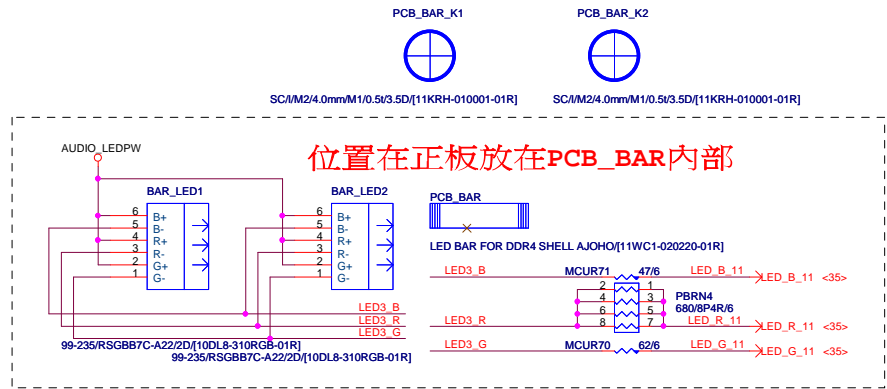
第一區 LED CONTROL

第二區 LED CONTROL



Note : Pulldown address is 0x8C

GIGABYTE™		
Title CPU / AUDIO / PCIE/REAR LED		
Size	Document Number	Rev
Custom	AB350-GAMING 3	1.01
Date	Thursday, January 19, 2017	Sheet 35 of 37



FOR 燈條 LED (LED_C放在PCB左邊板邊位置)

